

System Block Diagram

SYNC_MASTER=T18_MLB

SYNC_DATE=12/12/2007

NOTICE OF PROPRIETARY PROPERTY

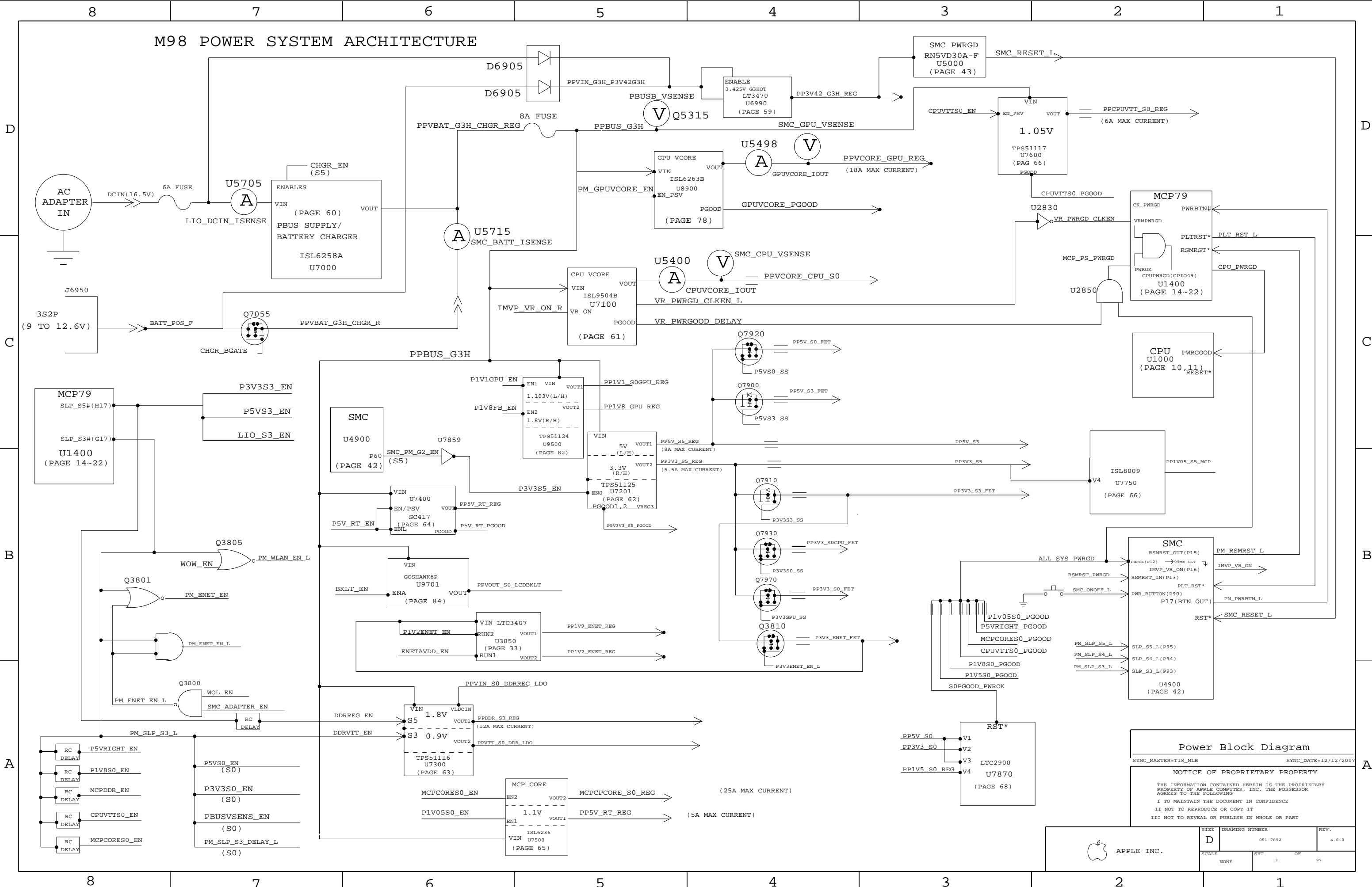
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	D	051-7892	A.0.0
SCALE		SHT	OF
NONE		2	97



APPLE INC.

SIZE	D	DRAWING NUMBER	051-7892	REV.	A.0.0
SCALE	NONE	SHT	3	OF	97

Power Block Diagram

SYNC_MASTER=T18_MLB

SYNC_DATE=12/12/2007

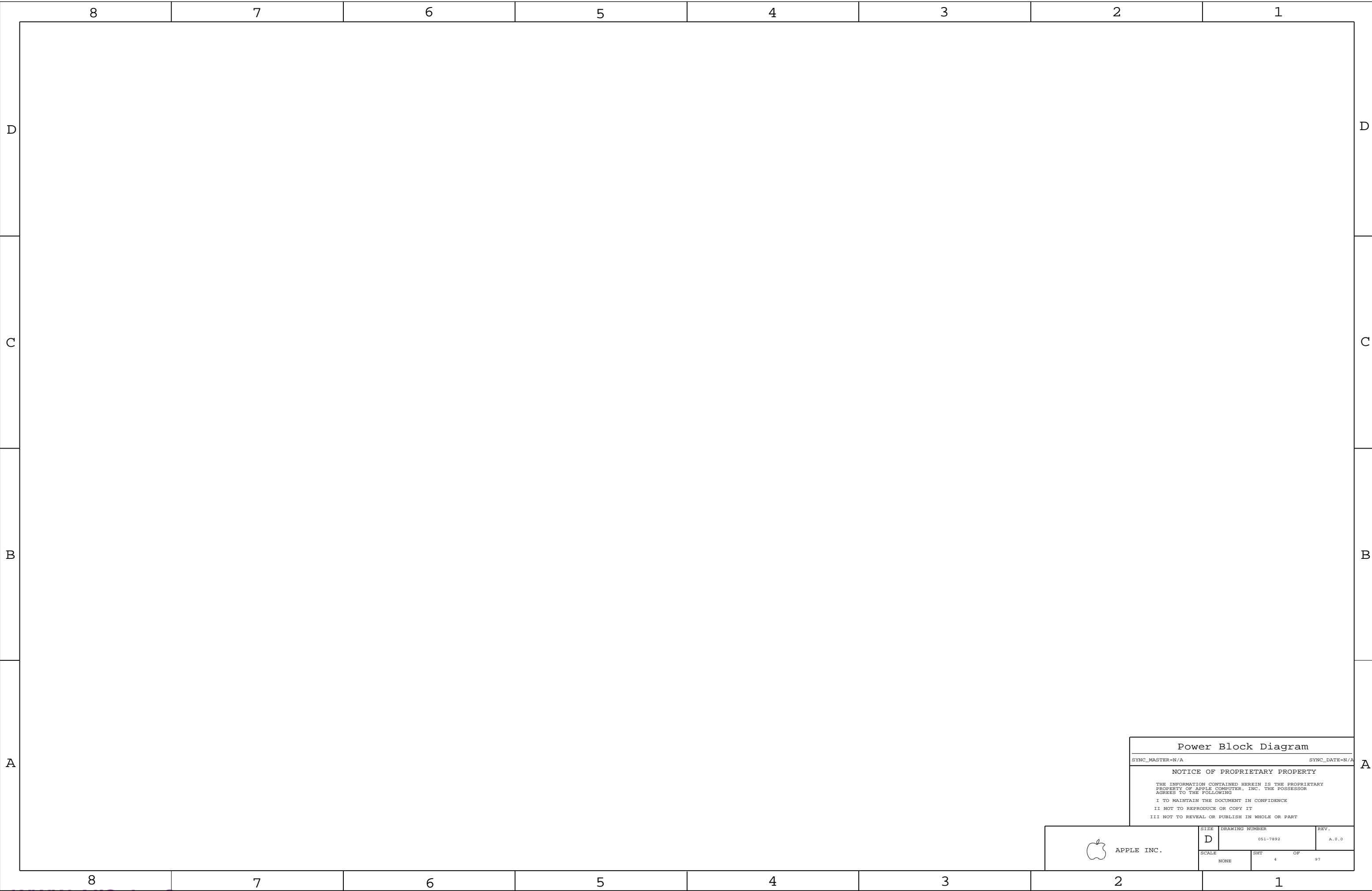
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Power Block Diagram			
SYNC_MASTER=N/A		SYNC_DATE=N/A	
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SCALE	SHT	OF	
NONE	4	97	

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9965	PCBA, 2.66GHZ, 256SAM_VRAM, HB_AUDIO, K19	K19_COMMON, DEVEL_BOM, EEE_6XN, CPU_2_66GHZ, FB_256_SAMSUNG
630-9966	PCBA, 2.66GHZ, 256HYN_VRAM, HB_AUDIO, K19	K19_COMMON, DEVEL_BOM, EEE_6XP, CPU_2_66GHZ, FB_256_HYNIX
630-9967	PCBA, 2.80GHZ, 512SAM_VRAM, HB_AUDIO, K19	K19_COMMON, DEVEL_BOM, EEE_6XQ, CPU_2_80GHZ, FB_512_SAMSUNG
630-9968	PCBA, 2.80GHZ, 512HYN_VRAM, HB_AUDIO, K19	K19_COMMON, DEVEL_BOM, EEE_6XR, CPU_2_80GHZ, FB_512_HYNIX
630-9969	PCBA, 3.06GHZ, 512SAM_VRAM, HB_AUDIO, K19	K19_COMMON, DEVEL_BOM, EEE_6XS, CPU_3_06GHZ, FB_512_SAMSUNG
630-9970	PCBA, 3.06GHZ, 512HYN_VRAM, HB_AUDIO, K19	K19_COMMON, DEVEL_BOM, EEE_6XT, CPU_3_06GHZ, FB_512_HYNIX
085-0736	K19 MLB DEVELOPMENT	K19_DEVEL_PVT

K19 BOM Groups

BOM GROUP	BOM OPTIONS
K19_COMMON	ALTERNATE, COMMON, K19, K19_COMMON1, K19_COMMON2, K19_PROGPARTS
K19_COMMON1	BOOT_MODE_USER, DPMUX_EN_S0, DP_CA_DET_EG_PLD, DP_ESD, EG_PWRSEQ_HW, EXTRACT_BUFF
K19_COMMON2	GMUX_lV8, GPUVID_1P00V, GPU_SS_INT, ISL6258A, MCP_B03, MCPSEQ_SMC, MIKEY, MUXGFX, SMC_DEBUG_YES, XDP
K19_DEVEL_ENG	BMON_ENG, DEBUG_ADC, GMUX_JTAG, LPCPLUS, VREFMRGN, XDP_CONN
K19_DEVEL_PVT	BMON_PROD, LPCPLUS, NO_VREFMRGN, XDP_CONN
K19_PROD	BMON_PROD, LPCPLUS_NOT, NO_VREFMRGN
K19_PROGPARTS	GMUX_PROG, BOOTROM_PROG, SMC_PROG, TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM4, VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM4, VRAM_256_HYNIX
FB_512_SAMSUNG	VRAM4, VRAM_512_SAMSUNG
FB_512_HYNIX	VRAM4, VRAM_512_HYNIX

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6XN]	CRITICAL	EEE_6XN
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6XP]	CRITICAL	EEE_6XP
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6XQ]	CRITICAL	EEE_6XQ
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6XR]	CRITICAL	EEE_6XR
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6XS]	CRITICAL	EEE_6XS
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6XT]	CRITICAL	EEE_6XT

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3761	1	IC,FDC,ELGLA,FHQ,2.66G,25W,1066,B0,3M,BGA	U1000	CRITICAL	CPU_2_66GHZ
337S3682	1	IC,FDT,SLGSH,FHQ,2.80G,35W,1066,B0,6M,BGA	U1000	CRITICAL	CPU_2_80GHZ
337S3744	1	IC,FDC,ELGLH,G0,3.06G,35W,1066,B0,6M,BGA	U1000	CRITICAL	CPU_3_06GHZ
338S0710	1	IC,MCP79MXT-B3,35X35MM,BGA1437	U1400	CRITICAL	MCP_B03
338S0694	1	IC,RTL8251CA-VB-QR,Q1QR TRANSCEIVER,48P LQFP	U3700	CRITICAL	
338S0654	1	IC,PWM43-E,13848 RVY/GMI 1.5NM/PCT-E,12	U4100	CRITICAL	
341S2384	1	IB,ENCORE I1, CVT063803-LQCC	U4800	CRITICAL	
338S0563	1	IC,SMC,H58/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2462	1	IC,SMC,DEVELOPMENT,K19	U4900	CRITICAL	SMC_PROG
341S2503	1	IC,PSOC +W/USB,56PIN,MLF,K19	U5701	CRITICAL	TPAD_PROG
335S0384	1	IC,32MBIT 8-PIN SPI SERIAL FLASH,S01CS	U6100	CRITICAL	BOOTROM_BLANK
341S2456	1	IC,EFI ROM,DEVELOPMENT,K19	U6100	CRITICAL	BOOTROM_PROG
338S0554	1	IC,GPU,55nm,NV G96-GS,BGA969,LFP	U8000	CRITICAL	
333S0507	4	IC,SGRAM,GDDR3,16Mx32,1000MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0483	4	IC,SGRAM,GDDR3,16Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX
333S0511	4	IC,SGRAM,GDDR3,32Mx32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0506	4	IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_HYNIX

Development BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-0736	1	K19 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM

BOM Configuration

SYNC_MASTER=DDR SYNC_DATE=12/18/2008

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SIZE DRAWING NUMBER REV.

D 051-7892 A.0.0

SCALE NONE

SHT 5 OF 97

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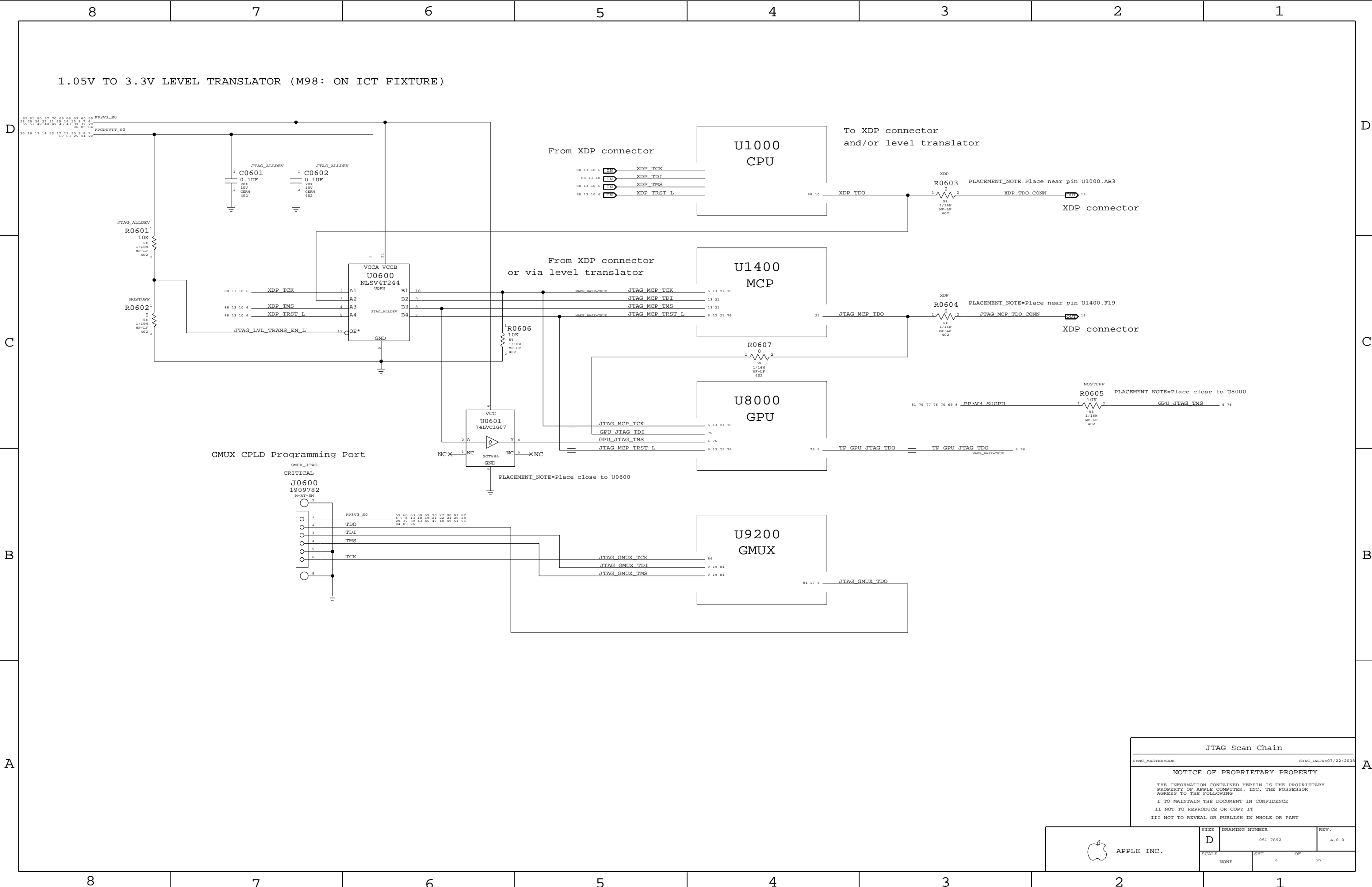
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JTAG Scan Chain

SYNC_MASTER=DDR

SYNC_DATE=07/22/2008


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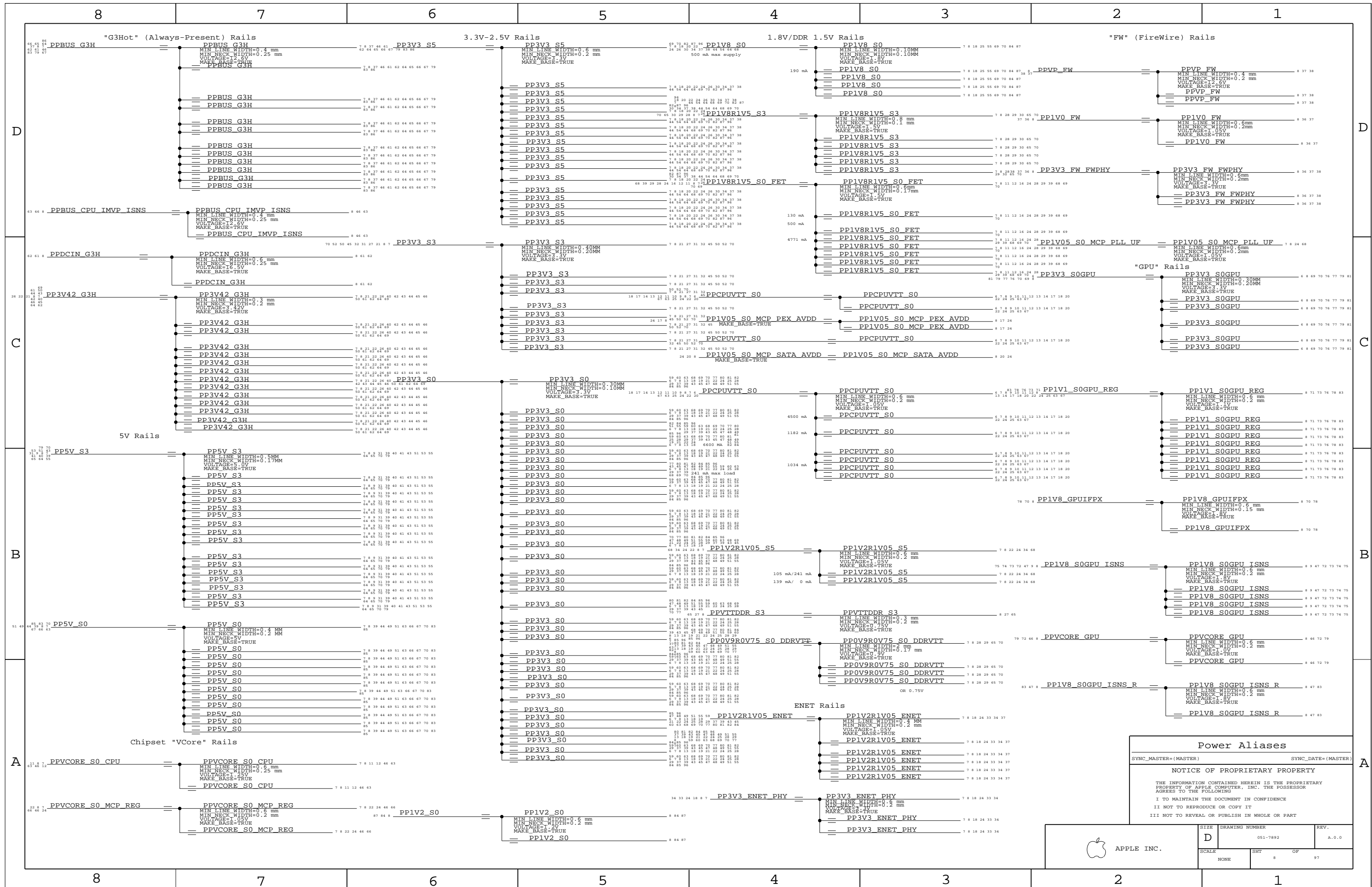
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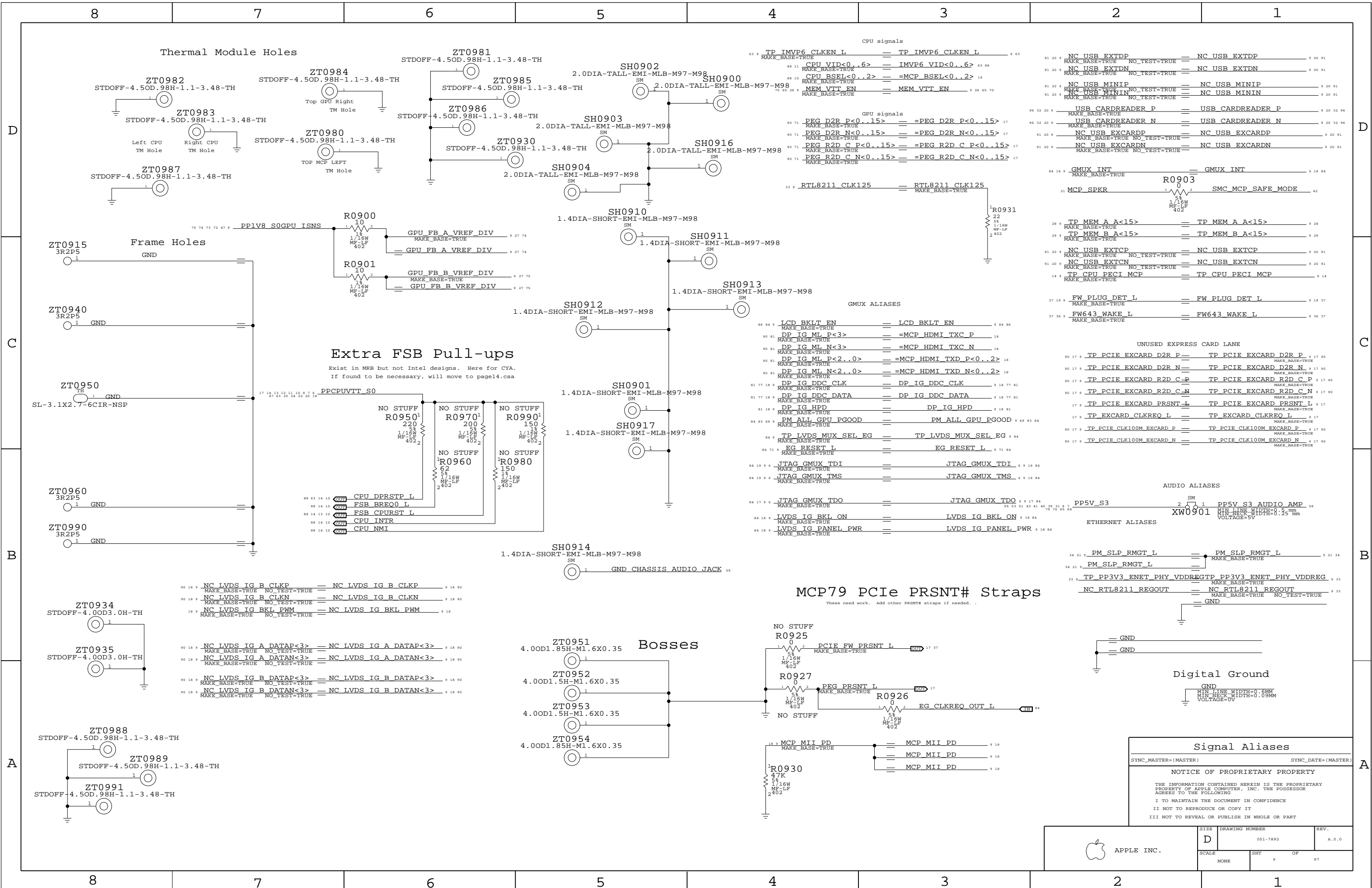
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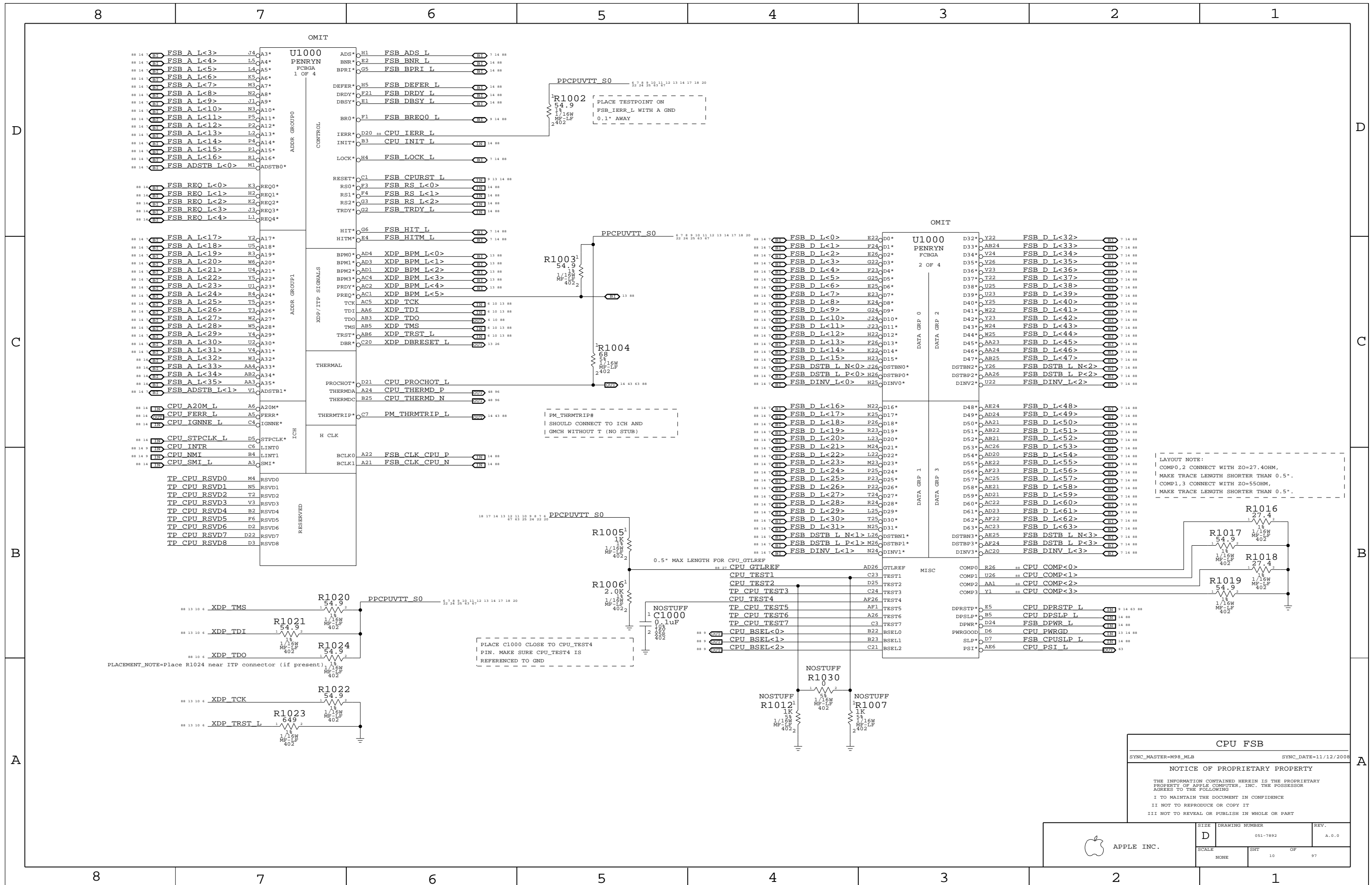
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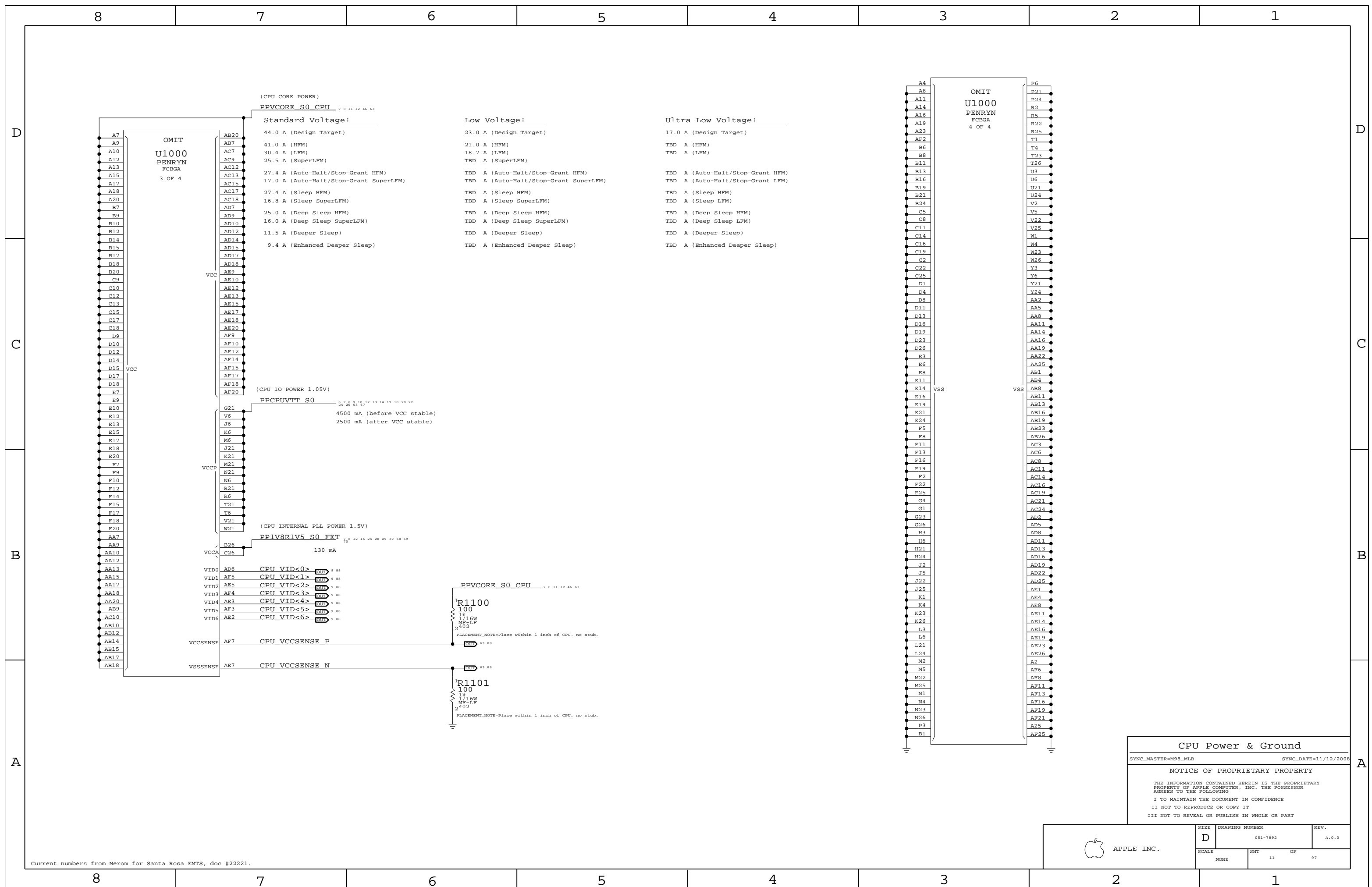
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	SCALE NONE	SHT 6	OF 97

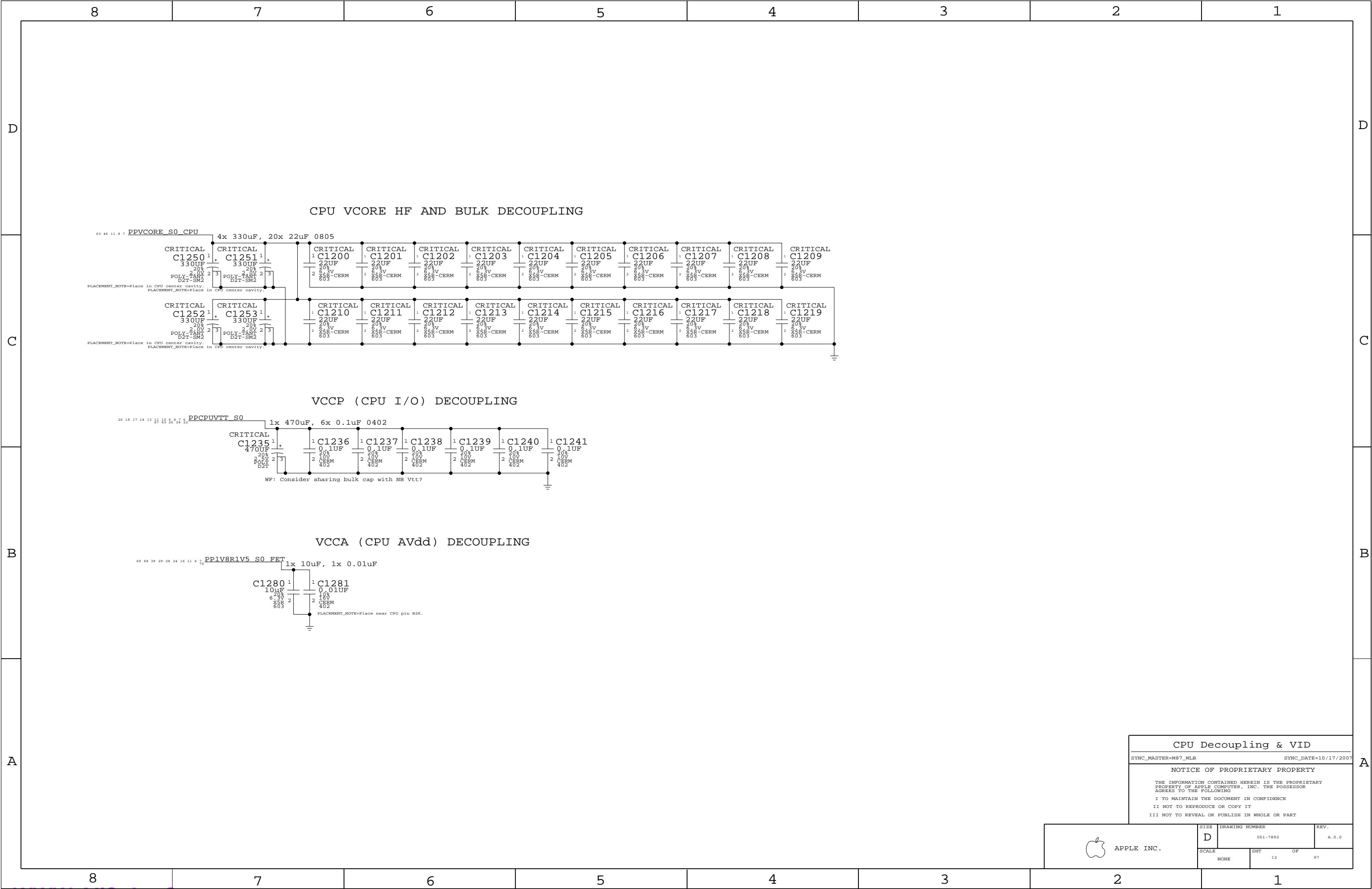
8	7	6	5	4	3	2	1
Functional Test Points							
Fan Connectors		SATA ODD Connectors		DC Power Connector		ICT Test Points	
FANCTEST		FANCTEST		FANCTEST		NO_TEST	
TRUE PP5V S0		TRUE PP5V SW ODD		TRUE PP18V5 DCIN FUSE		NC AUD LO1 N L	
TRUE FAN LT PWM		TRUE SMC ODD DETECT		TRUE ADAPTER SENSE		NC AUD LO1 P L	
TRUE FAN LT TACH		TRUE SATA ODD R2D P		TRUE GND		NC USB 10N	
TRUE FAN RT PWM		TRUE SATA ODD R2D N		TRUE GND		NC USB 10P	
TRUE FAN RT TACH		TRUE SATA ODD D2R C N		TRUE GND		NC ENET INTR L	
TRUE GND		TRUE SATA ODD D2R C P		TRUE GND		NC ENET PWRDWN L	
		TRUE GND				MAKE_BASE=TRUE	
LVDS Connector		Keyboard Connector		Battery Connector			
FANCTEST		FANCTEST		FANCTEST			
TRUE PP3V3 S0		TRUE PP3V3 S3		TRUE PPVBAT G3H CONN		NC LPC DRQ0 L	
TRUE PP3V3 SW LCD		TRUE PP3V42 G3H		TRUE SMBUS SMC BSA SCL		TP MEM A CKE<3..2>	
TRUE PPVOUT S0 LCDBKLT		TRUE WS KBD1		TRUE SMBUS SMC BSA SDA		NC MEM A CLK2N	
		TRUE WS KBD2		TRUE SYS DETECT L		NC MEM A CLK3N	
		TRUE WS KBD3		TRUE GND		NC MEM A CLK3P	
		TRUE WS KBD4				NC MEM A CLK4P	
		TRUE WS KBD5				NC MEM A CS L<3>	
		TRUE WS KBD6				TP MEM A ODT<3..2>	
		TRUE WS KBD7				MAKE_BASE=TRUE	
		TRUE WS KBD8					
		TRUE WS KBD9				NC MEM B CKE<2>	
		TRUE WS KBD10				NC MEM B CLK3P	
		TRUE WS KBD11				NC MEM B CLK3P	
		TRUE WS KBD12				NC MEM B CLK4N	
		TRUE WS KBD13				NC MEM B CLK4P	
		TRUE WS KBD14				NC MEM B CLK5N	
		TRUE WS KBD15 CAP				NC MEM B ODT<2>	
		TRUE WS KBD16 NUM				NC MLB RAM SIZE	
		TRUE WS KBD17				NC P7 7	
		TRUE WS KBD18				TP PCI AD<31..8>	
		TRUE WS KBD19				MAKE_BASE=TRUE	
		TRUE WS KBD20					
		TRUE WS KBD21				NC PCI CLK0	
		TRUE WS KBD22				NC PCI CLK1	
		TRUE WS KBD23				NC PCI DEVSEL L	
		TRUE WS KBD ONOFF L				NC PCI FRAME L	
		TRUE WS LEFT SHIFT KBD				NC PCI GNT0 L	
		TRUE WS LEFT OPTION KBD				NC PCI GNT1 L	
		TRUE WS CONTROL KBD				NC PCI INTW L	
		TRUE KBDLED ANODE				NC PCI INTX L	
						NC PCI INTZ L	
						NC PCI IRDY L	
						NC PCI PERR L	
						NC PCI RESET1 L	
						NC PCI SERR L	
						NC PCI STOP L	
						NC PCI TRDY L	
						NC PCIE CLK100M PE4N	
						NC PCIE CLK100M PE4P	
						NC PCIE CLK100M PE5N	
						NC PCIE CLK100M PE5P	
						NC PCIE CLK100M PE6P	
						NC PCIE PE4 D2RN	
						NC PCIE PE4 R2D CN	
						NC PE4 PRSNT L	
						NC PSOC P1 3	
						NC PSOC SDA	
						NC SATA C D2RP	
						NC SATA C R2D CN	
						NC SATA C R2D CP	
						NC SATA D D2RN	
						NC SATA D D2RP	
						NC SB A20GATE	
						MAKE_BASE=TRUE	
						TRUE	











CPU Decoupling & VID

SYNC_MASTER=M87_MLB

SYNC_DATE=10/17/2007


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	SCALE NONE	SHT 12	OF 97

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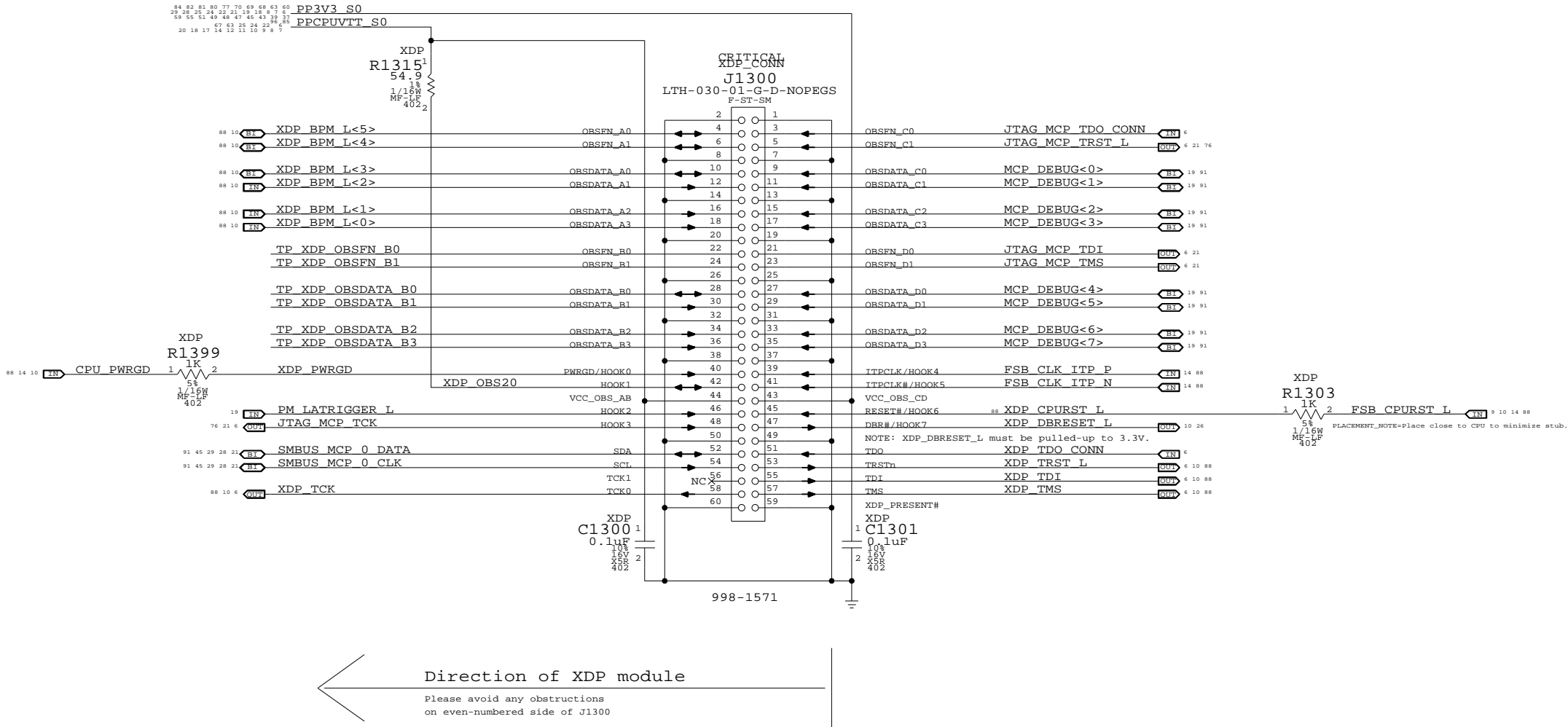
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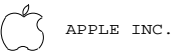
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout

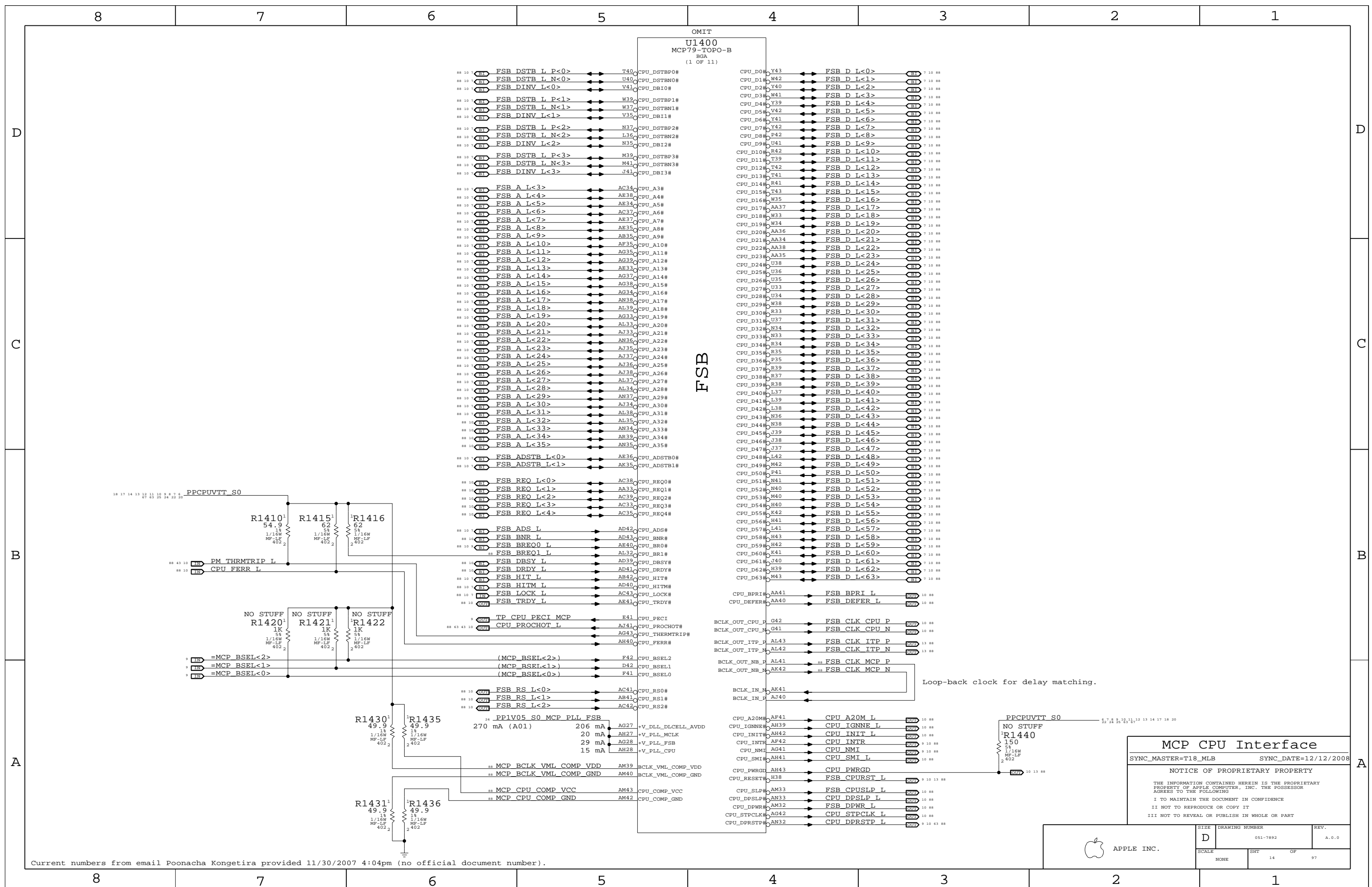


eXtended Debug Port (MiniXDP)		
SYNC_MASTER=M98_MLB		SYNC_DATE=11/12/2008
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SCALE	SHT	OF
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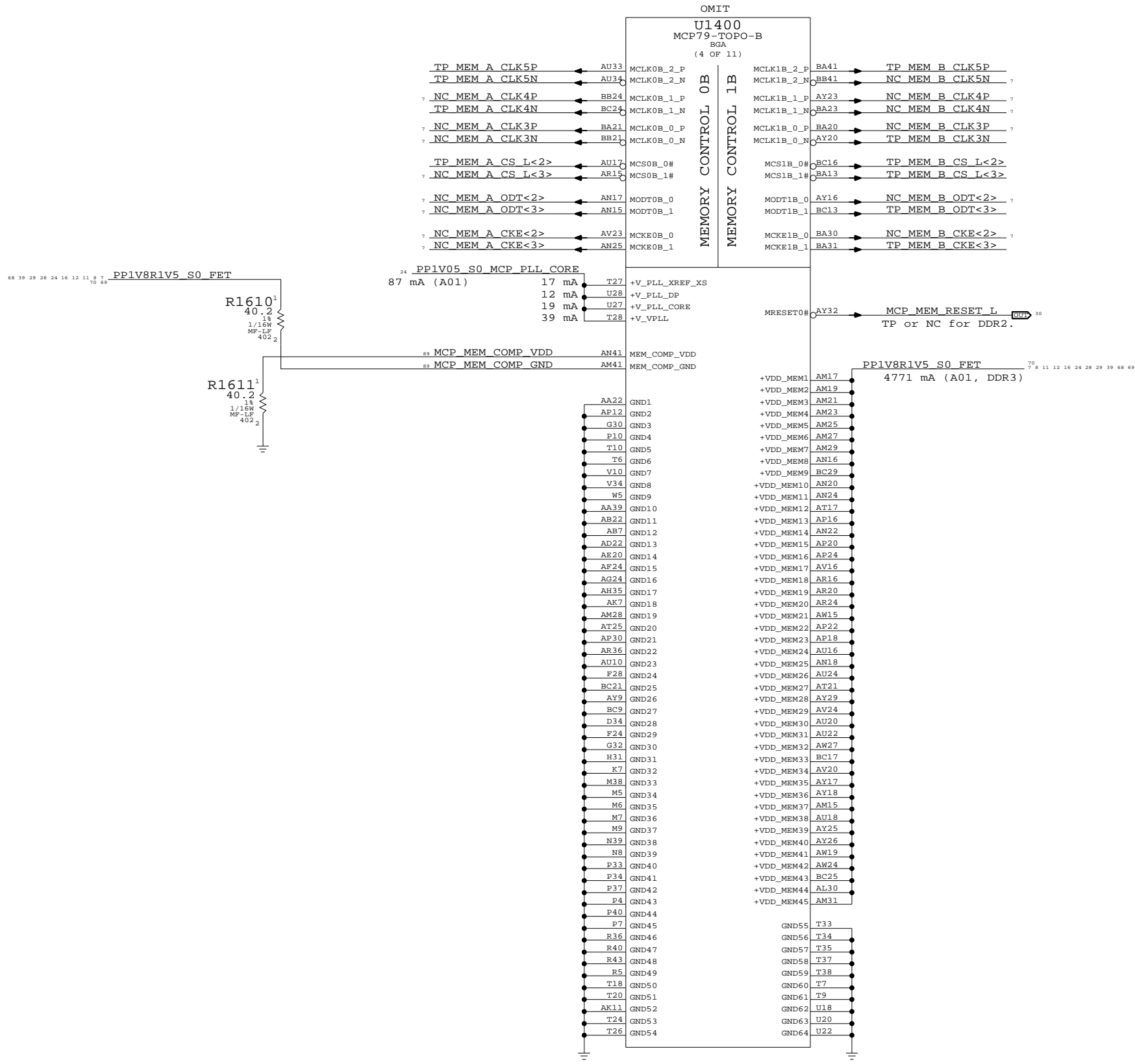
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Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Memory Misc

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

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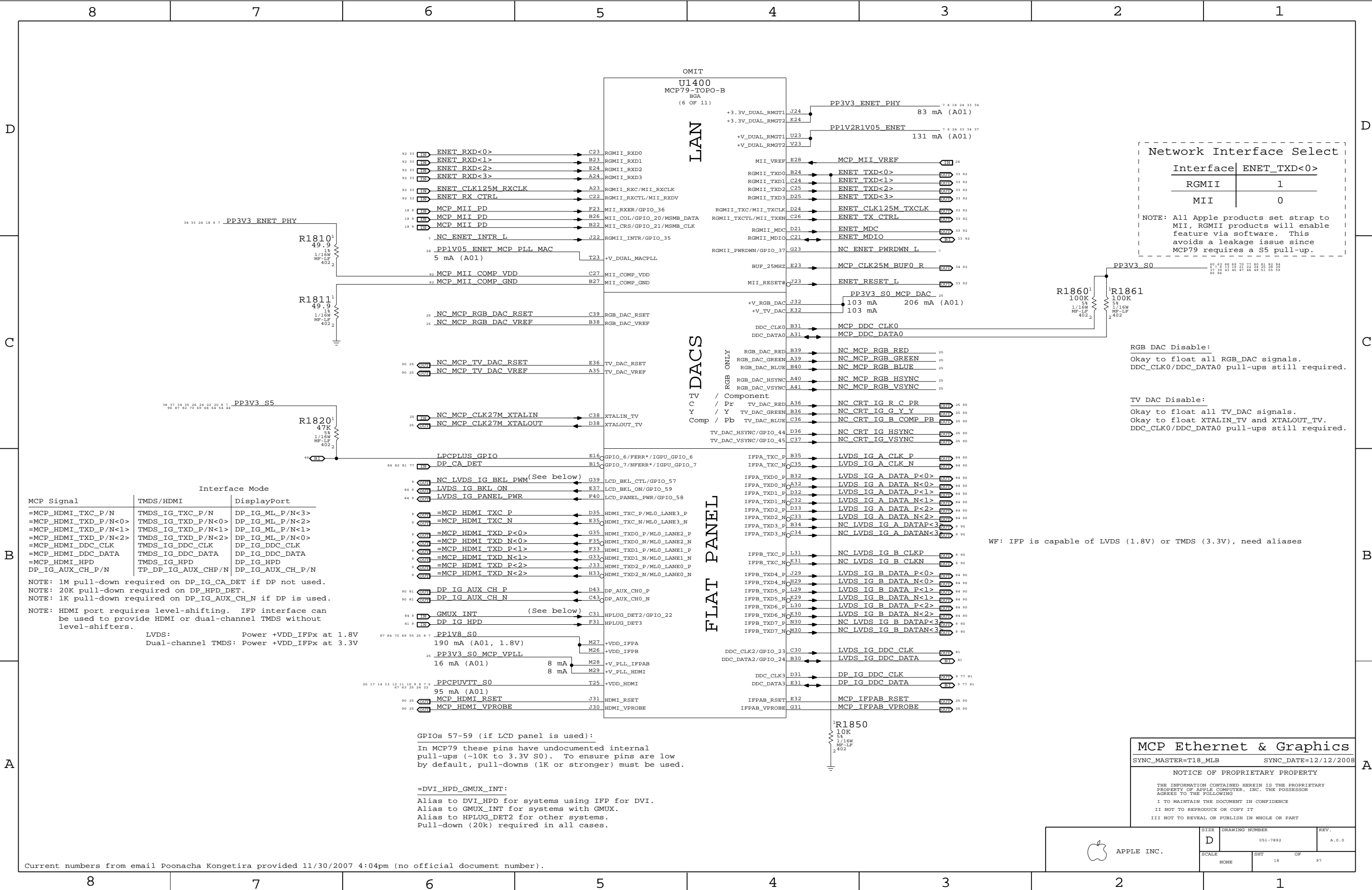
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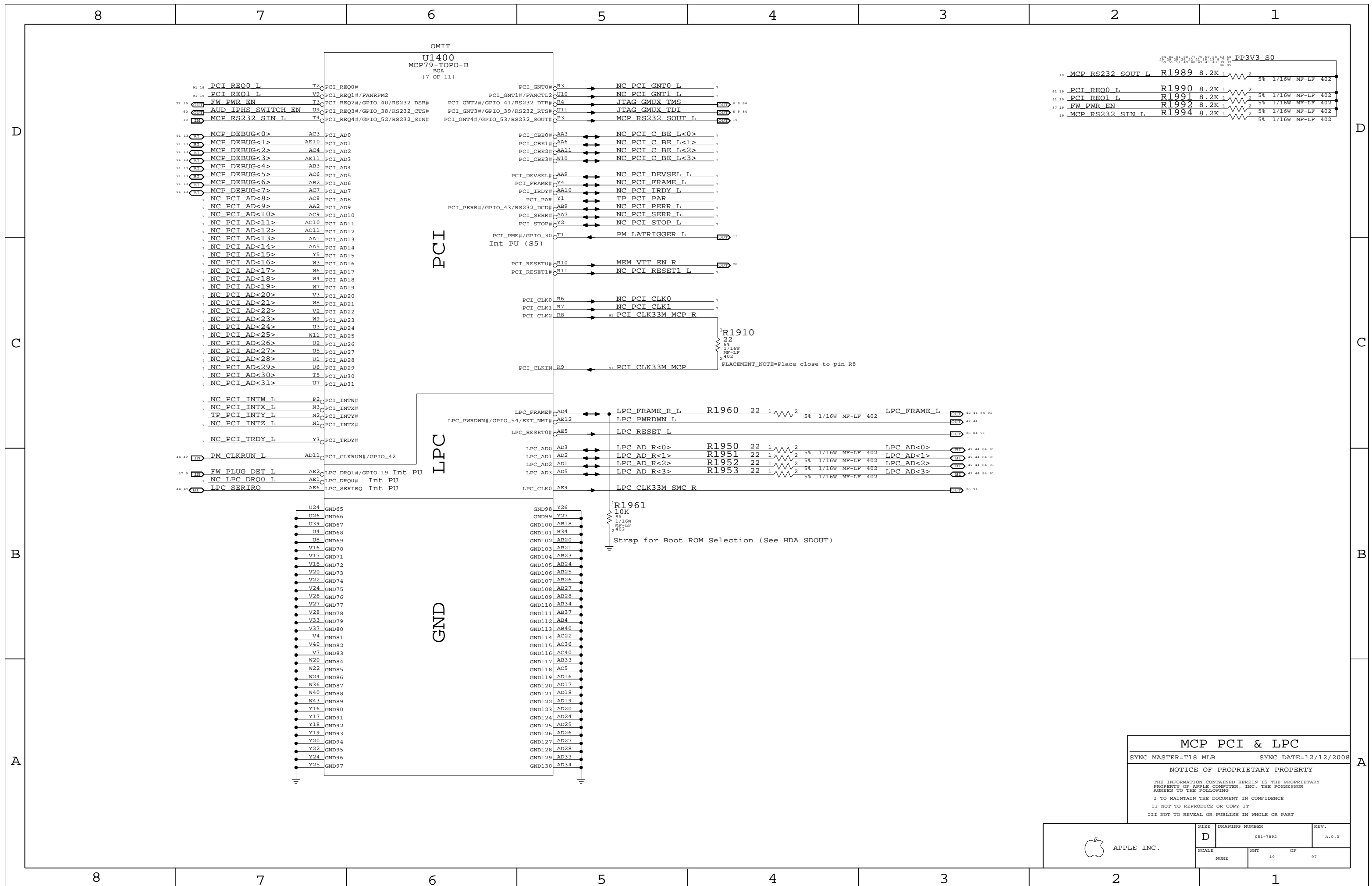
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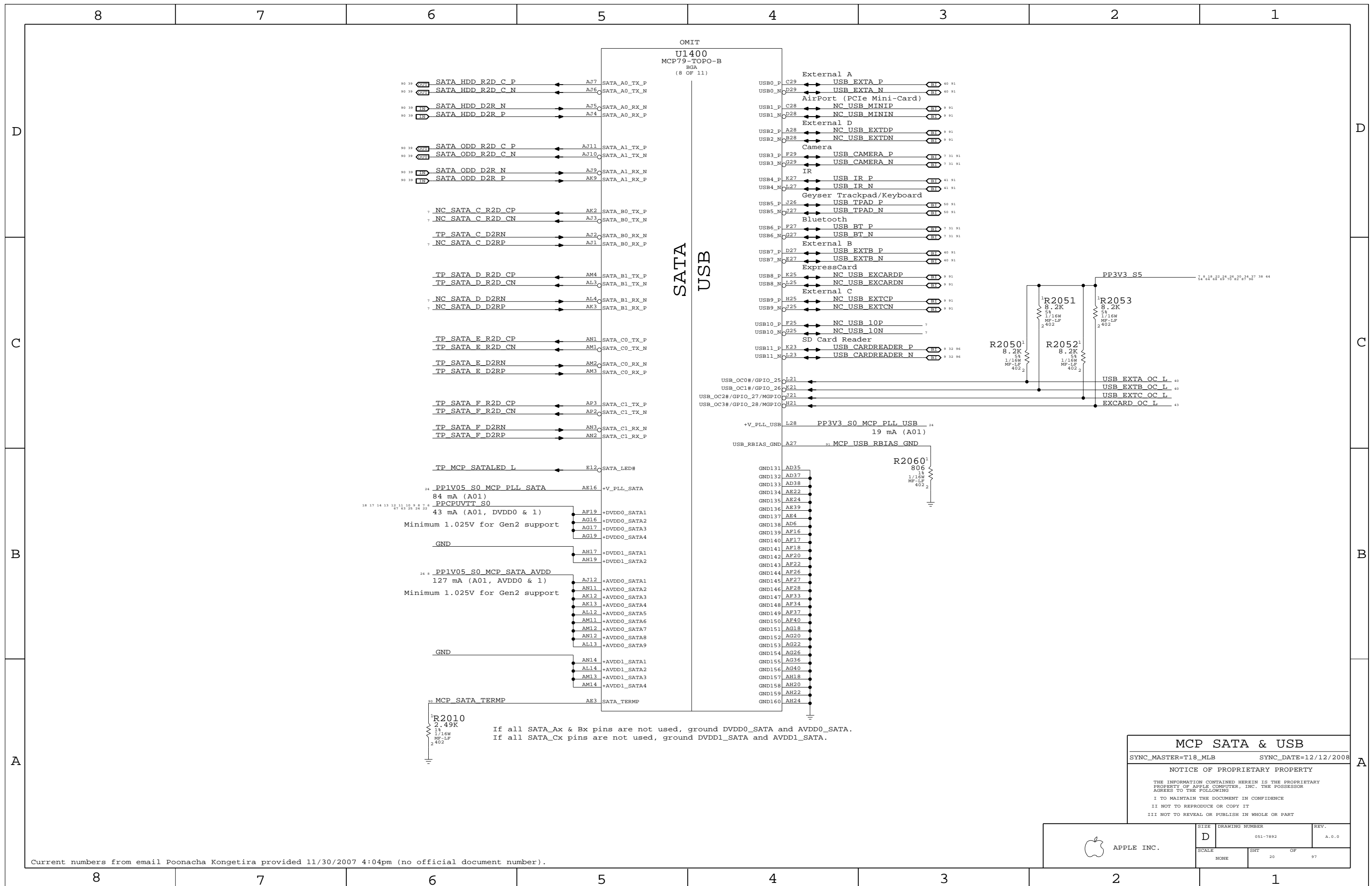
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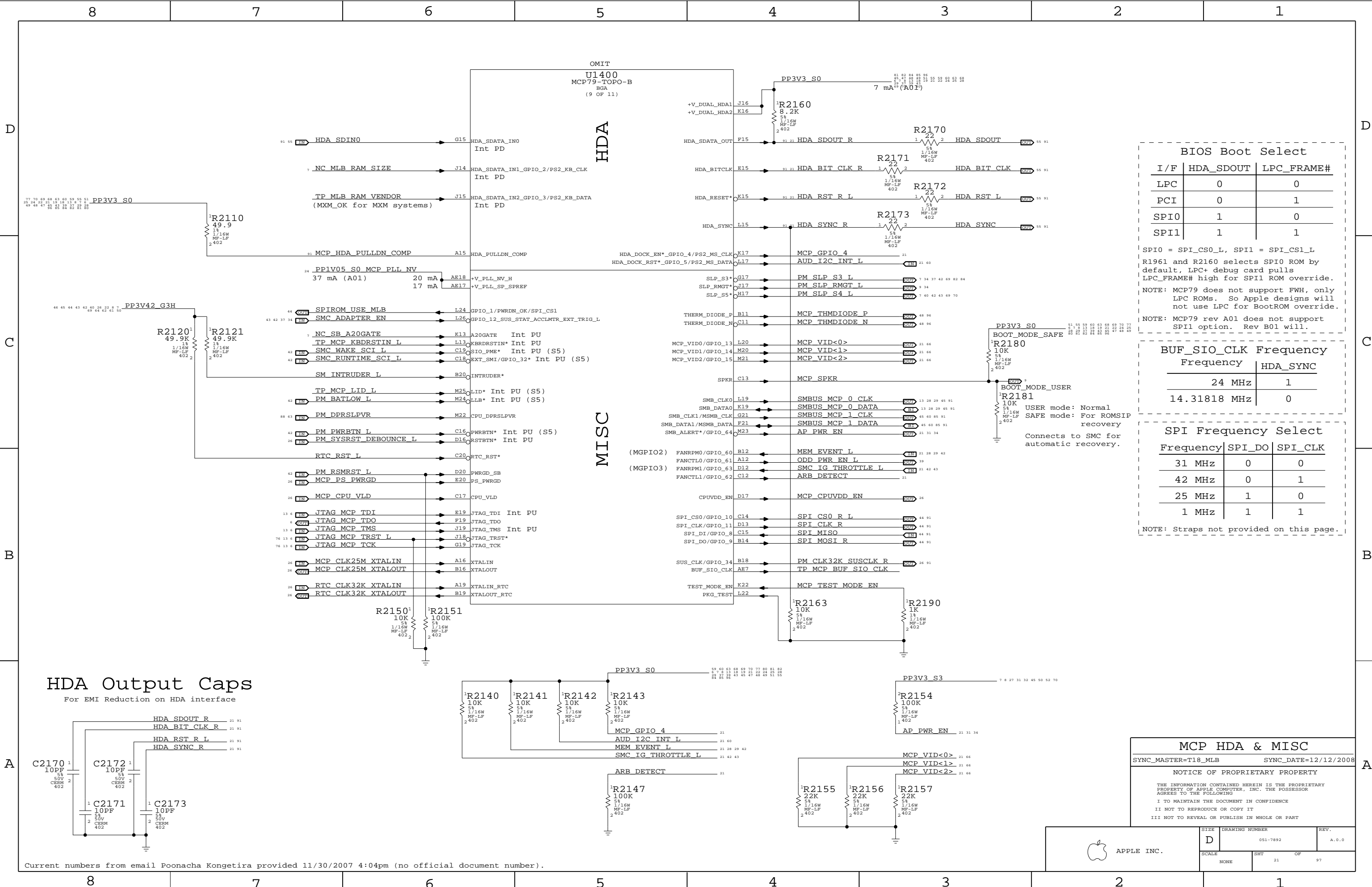
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BIOS Boot Select		
I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L
R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.
NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.
NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

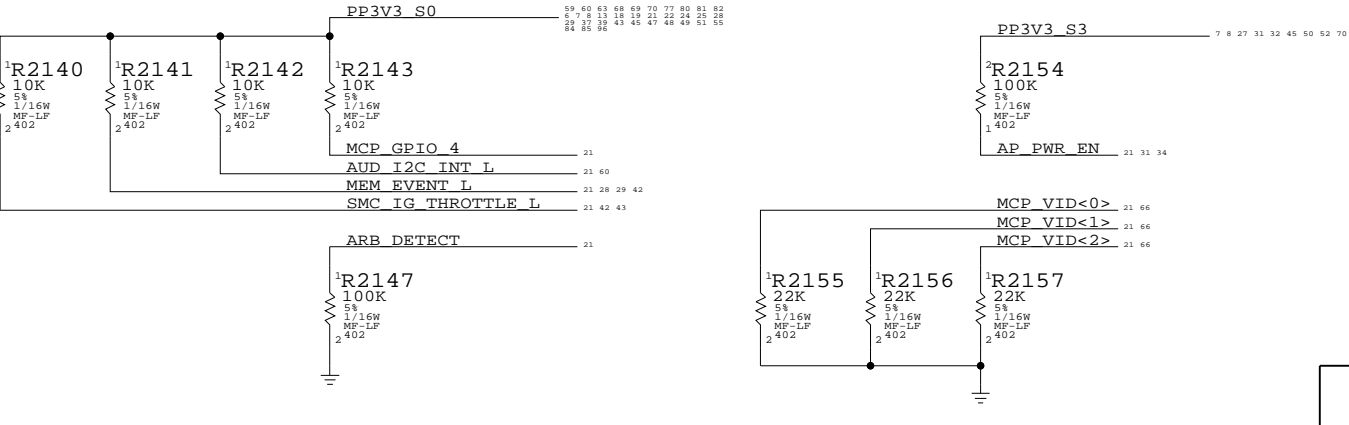
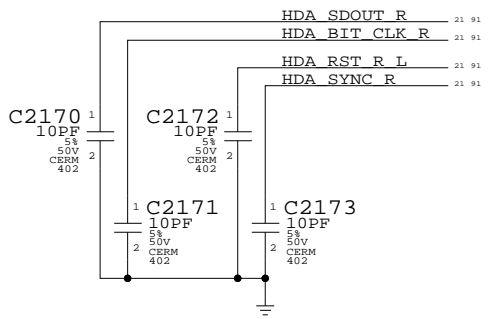
BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select		
Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface



MCP HDA & MISC

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DRAWING NUMBER

051-7892

REV.

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SCALE

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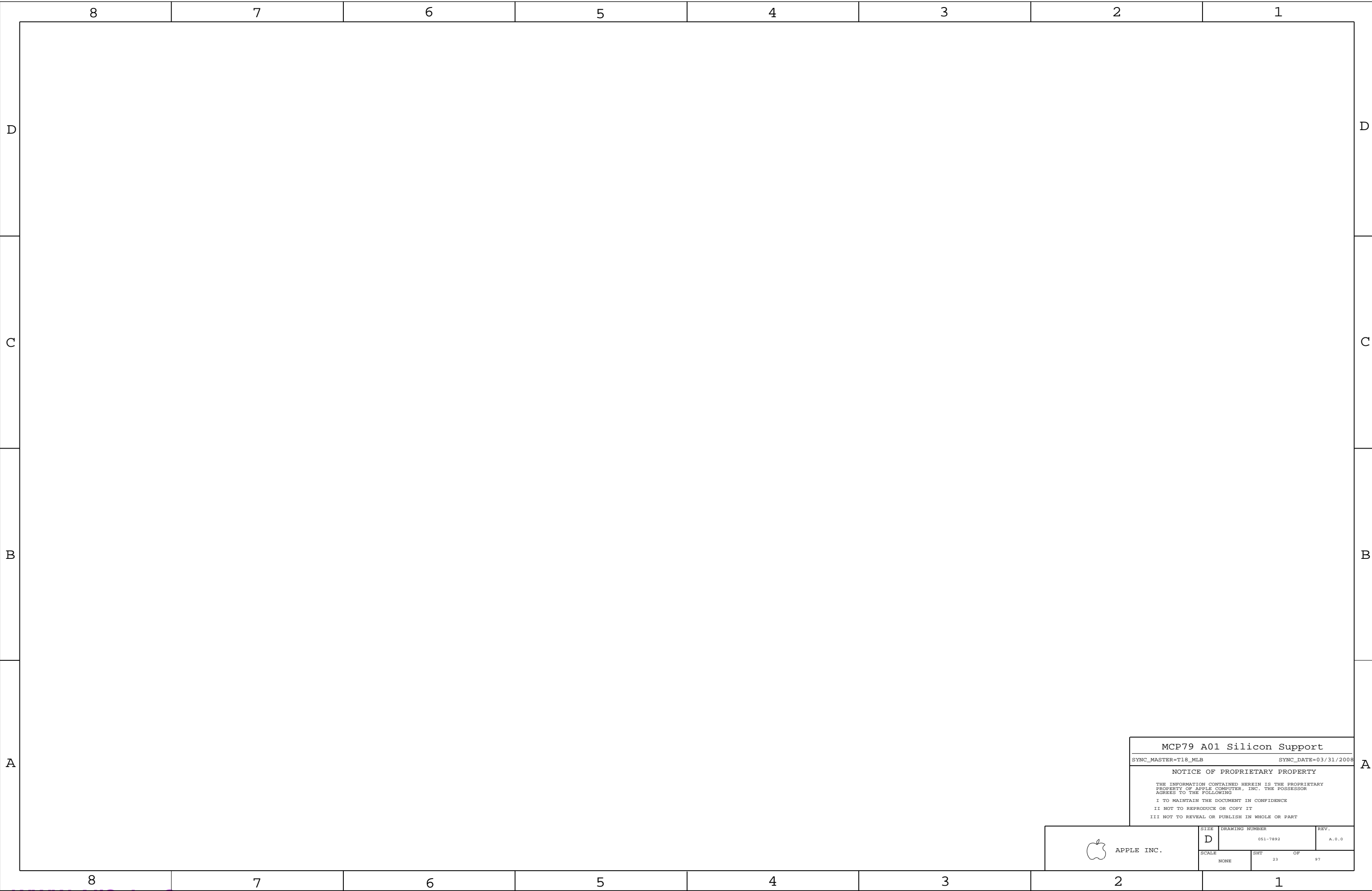
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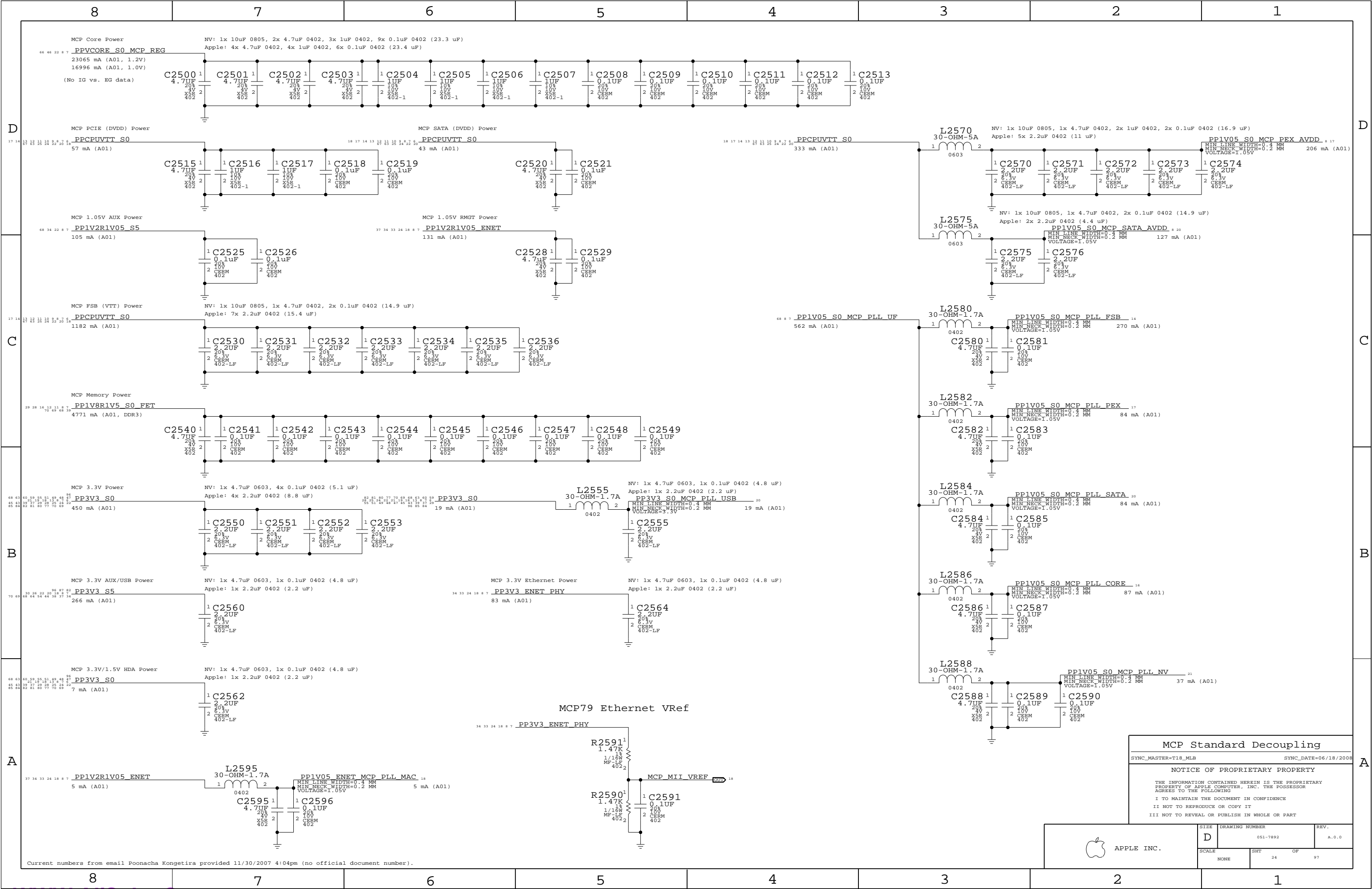
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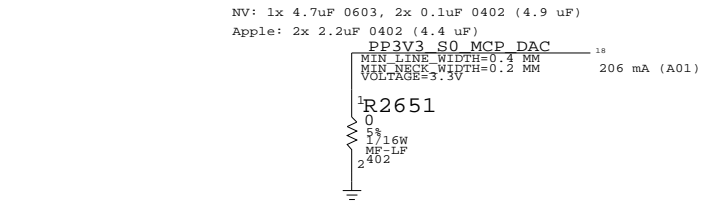
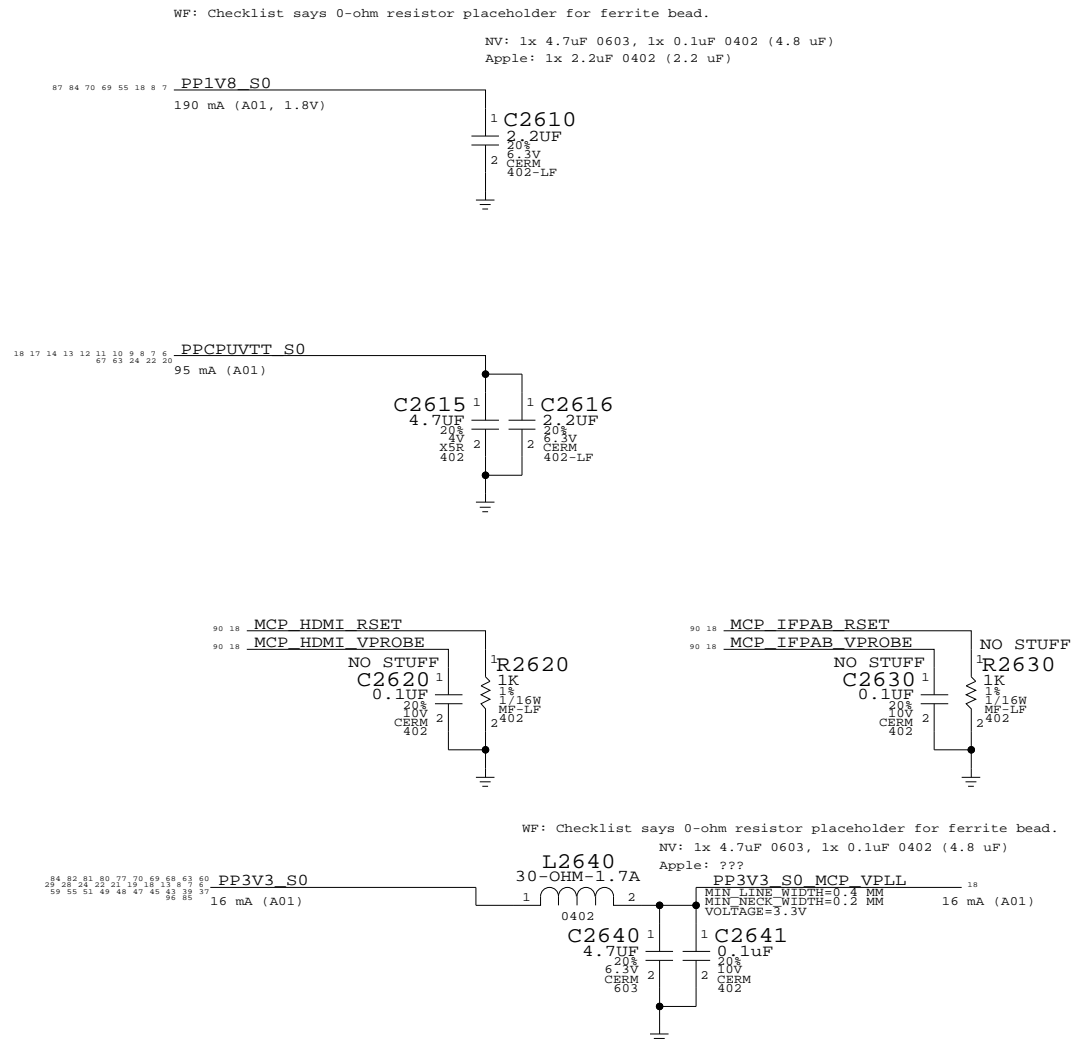
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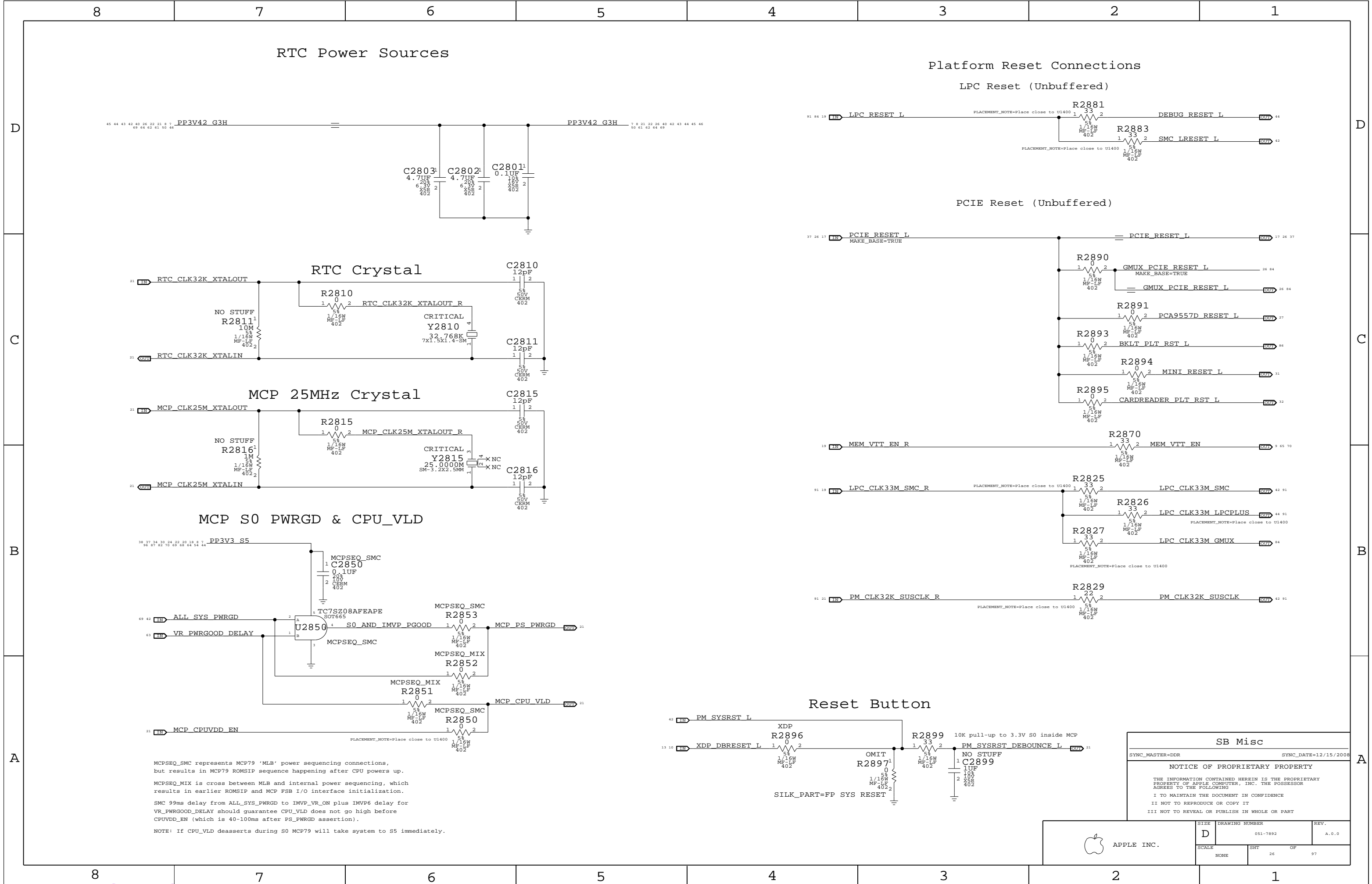








25	18	NC MCP RGB RED	—	NC MCP RGB RED	18	25	
				MAKE_BASE=TRUE NO_TEST=TRUE	18	25	
25	18	NC MCP RGB GREEN	—	NC MCP RGB GREEN	18	25	
				MAKE_BASE=TRUE NO_TEST=TRUE	18	25	
25	18	NC MCP RGB BLUE	—	NC MCP RGB BLUE	18	25	
				MAKE_BASE=TRUE NO_TEST=TRUE	18	25	
25	18	NC MCP RGB HSYNC	—	NC MCP RGB HSYNC	18	25	
				MAKE_BASE=TRUE NO_TEST=TRUE	18	25	
25	18	NC MCP RGB VSYNC	—	NC MCP RGB VSYNC	18	25	
				MAKE_BASE=TRUE NO_TEST=TRUE	18	25	
90	25	18	NC CRT IG R C PR	—	NC CRT IG R C PR	18	25
				MAKE_BASE=TRUE NO_TEST=TRUE	18	25	
90	25	18	NC CRT IG G Y Y	—	NC CRT IG G Y Y	18	25
				MAKE_BASE=TRUE NO_TEST=TRUE	18	25	
90	25	18	NC CRT IG B COMP PB	—	NC CRT IG B COMP PB	18	25
				MAKE_BASE=TRUE NO_TEST=TRUE	18	25	
90	25	18	NC CRT IG HSYNC	—	NC CRT IG HSYNC	18	25
				MAKE_BASE=TRUE NO_TEST=TRUE	18	25	
90	25	18	NC CRT IG VSYNC	—	NC CRT IG VSYNC	18	25
				MAKE_BASE=TRUE NO_TEST=TRUE	18	25	
25	18	NC MCP RGB DAC RSET	—	NC MCP RGB DAC RSET	18	25	
				MAKE_BASE=TRUE NO_TEST=TRUE	18	25	
25	18	NC MCP RGB DAC VREF	—	NC MCP RGB DAC VREF	18	25	
				MAKE_BASE=TRUE NO_TEST=TRUE	18	25	
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				MAKE_BASE=TRUE NO_TEST=TRUE	18	25	
90	25	18	NC MCP TV DAC VREF	—	NC MCP TV DAC VREF	18	25
				MAKE_BASE=TRUE NO_TEST=TRUE	18	25	
25	18	NC MCP CLK27M XTALIN	—	NC MCP CLK27M XTALIN	18	25	
				MAKE_BASE=TRUE NO_TEST=TRUE	18	25	
25	18	NC MCP CLK27M XTALOUT	—	NC MCP CLK27M XTALOUT	18	25	
				MAKE_BASE=TRUE NO_TEST=TRUE	18	25	



Page Notes

Power aliases required by this page:

```
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF
```

Signal aliases required by this page:

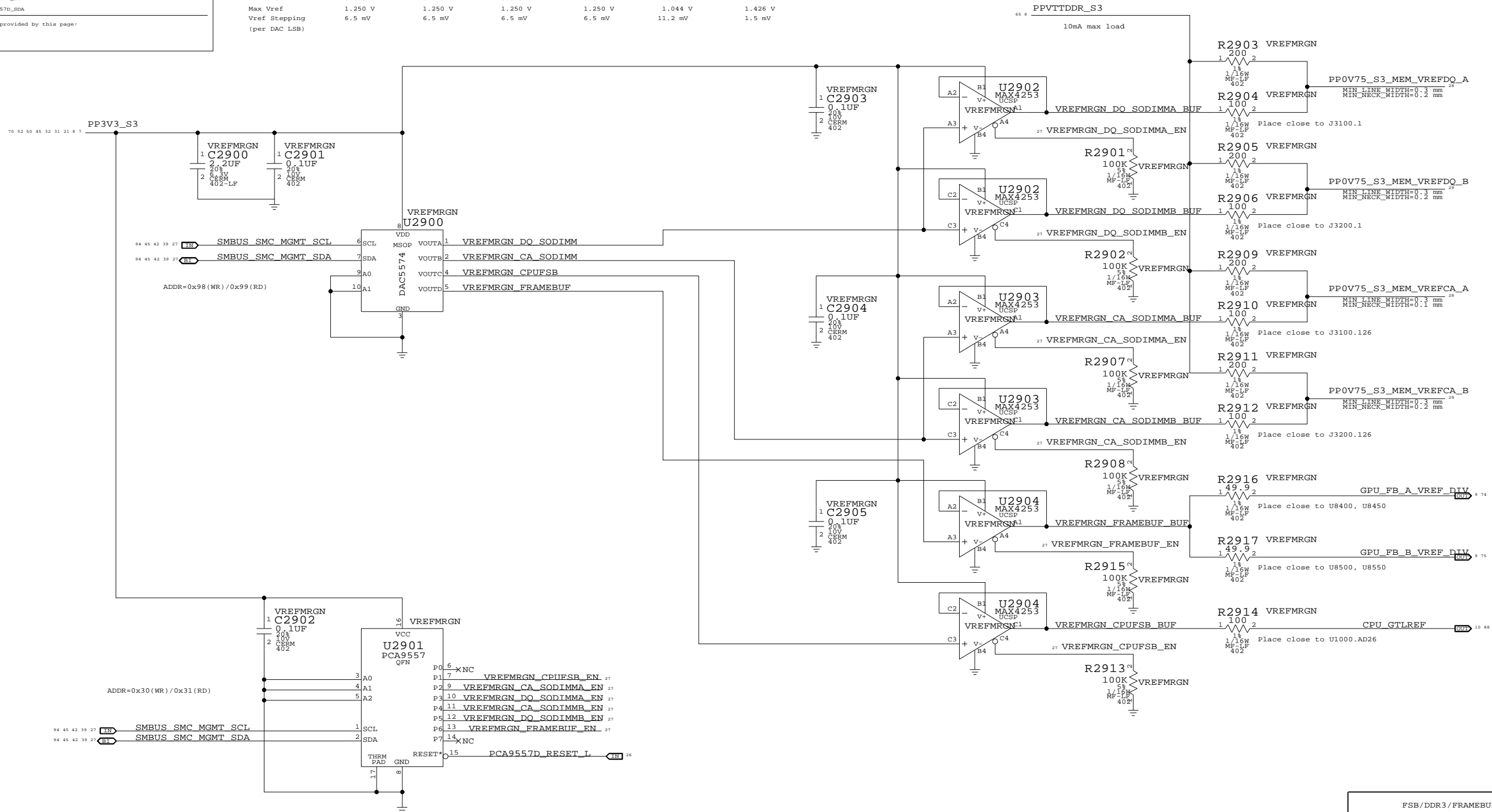
```
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA
```

BOM options provided by this page:

VREFMRGN
NO_VREFMRGN

	MEM A VREF DQ		MEM A VREF CA		MEM B VREF DQ		MEM B VREF CA		CPU FSB VREF	FRAME BUFFER VREF
DAC channel	A	B	A	B	C	D				
Min DAC code	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00		
Max DAC code	0x87	0x87	0x87	0x87	0x87	0x55	0xFF			
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA	-59.04 mA			
Max source I	5 mA	5 mA	5 mA	5 mA	5 mA	0.52 mA	51.15 mA			
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V	1.248 V			
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V	1.042 V			
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V	1.426 V			
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV	1.5 mV			

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



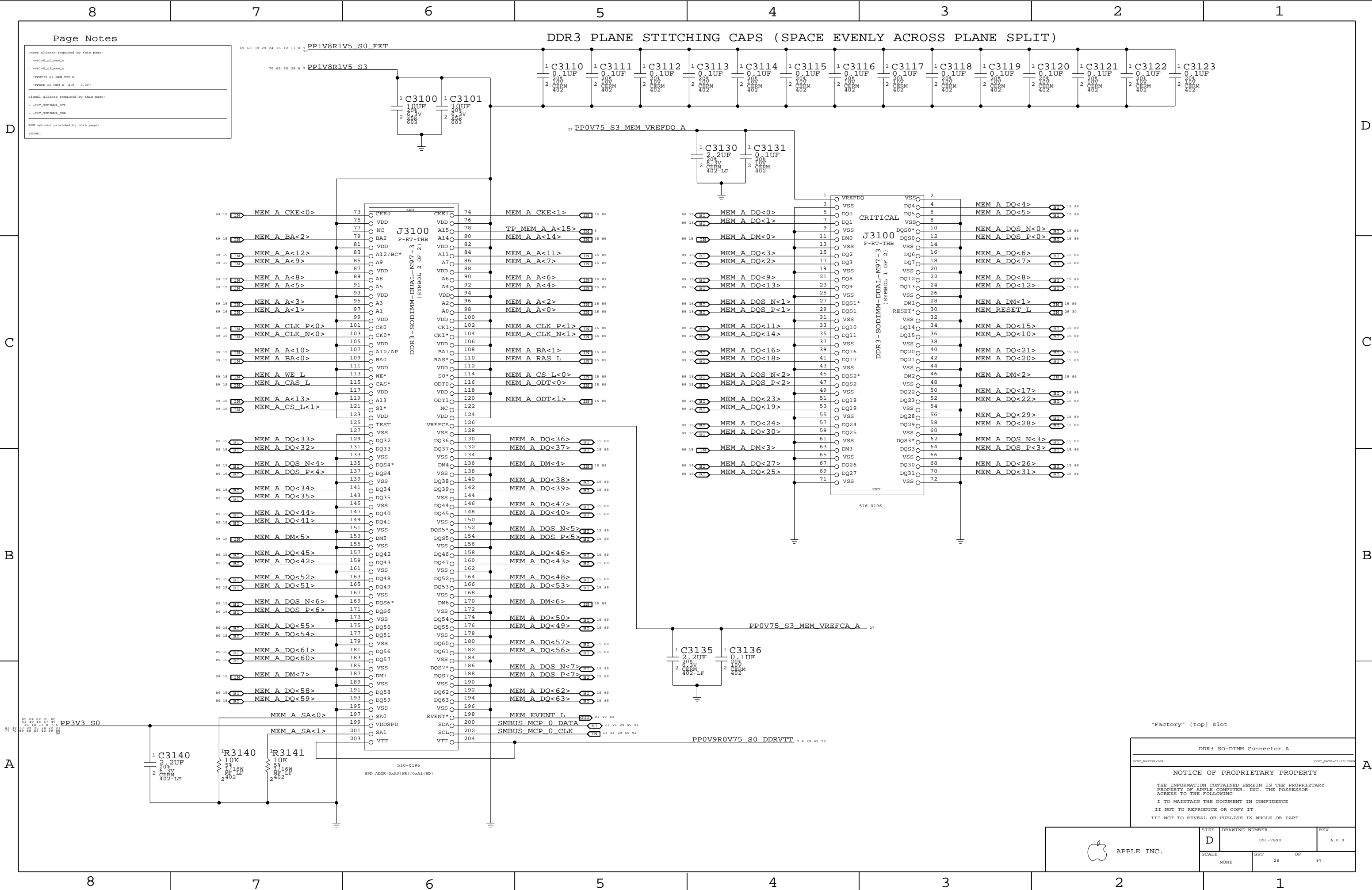
Required zero ohm resistors when no VREF margining circuit stuffed

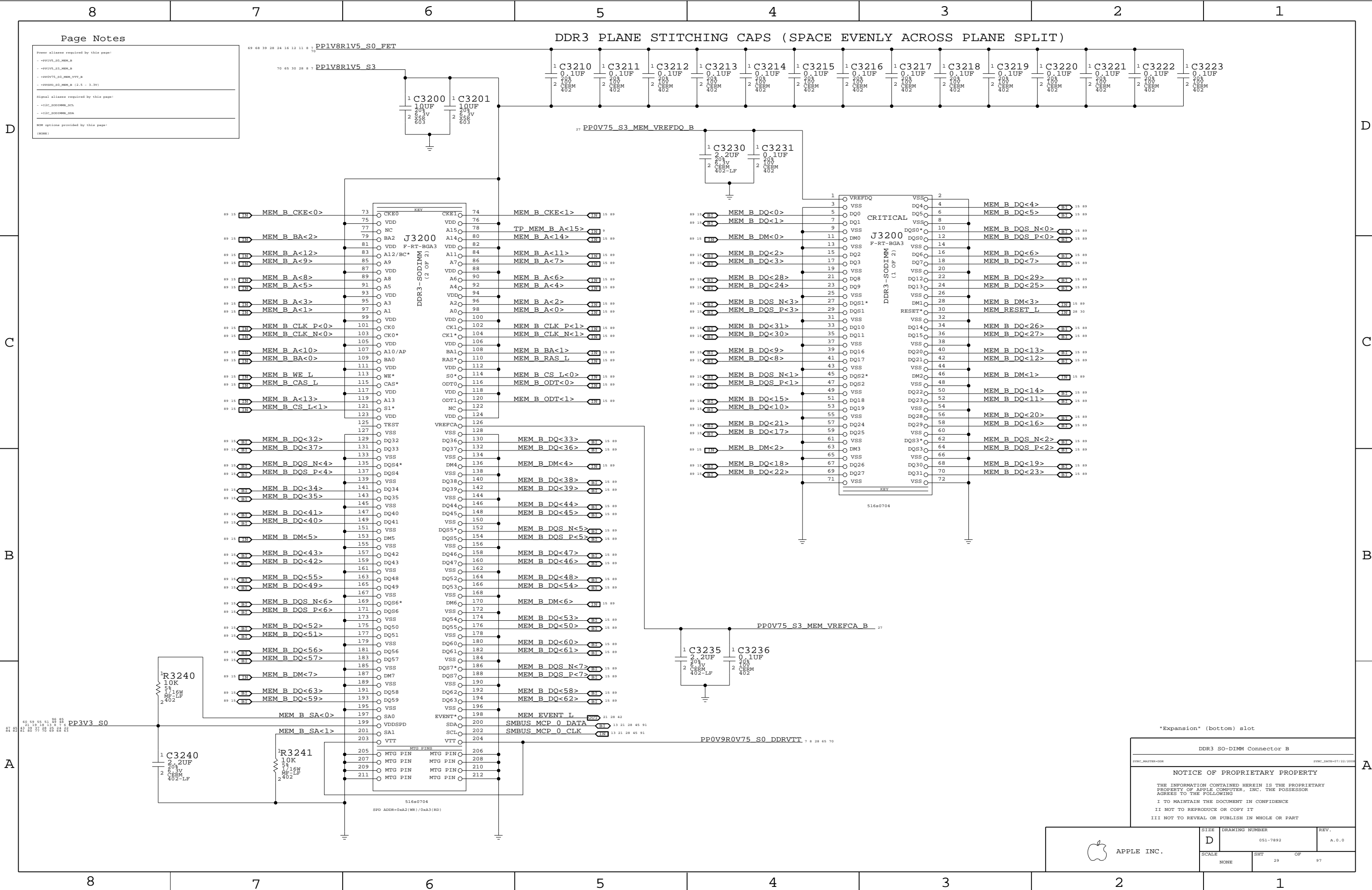
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

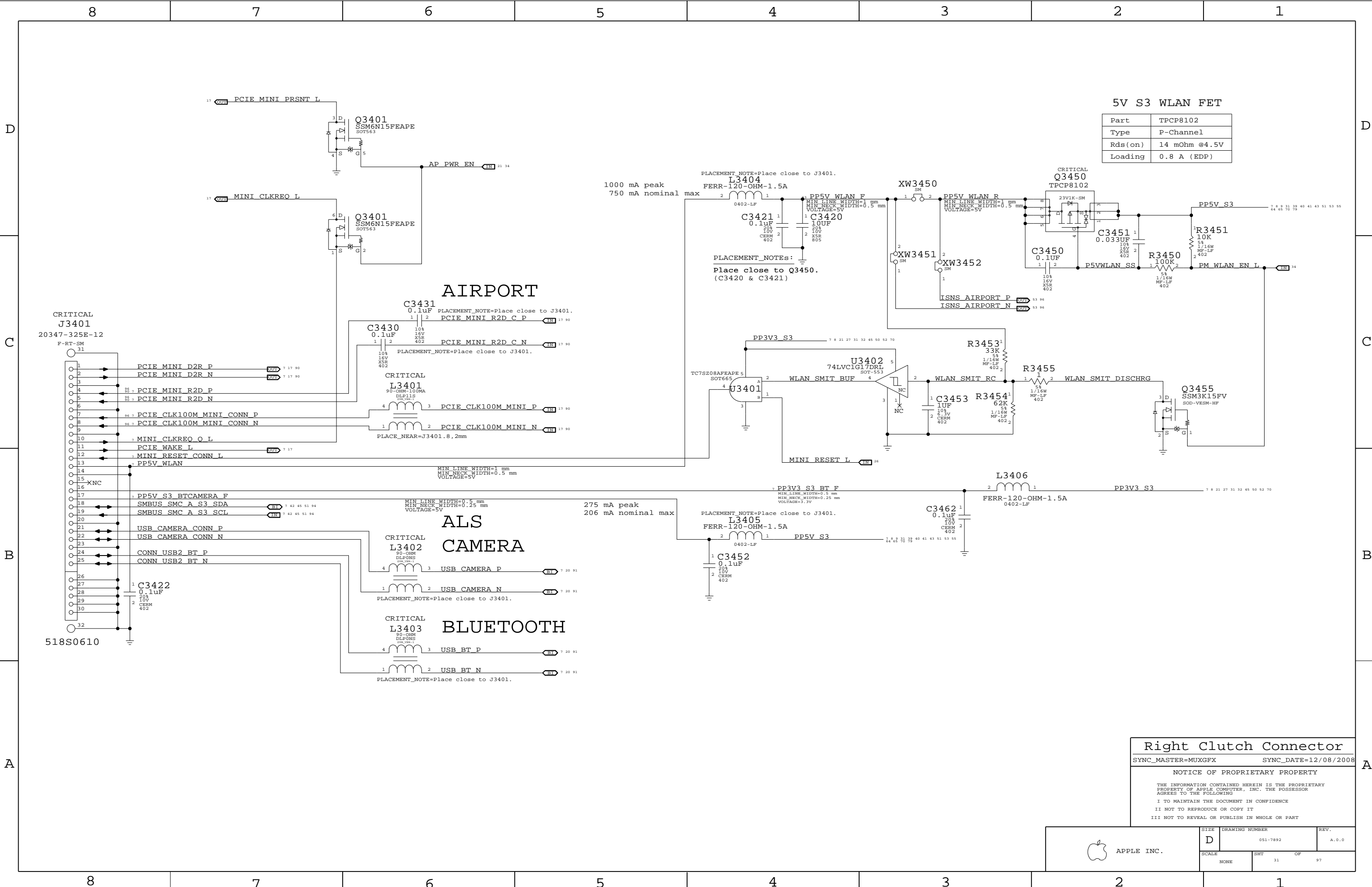
F5B/DDR3/FRAMEBUF Vref Margining	
SYNC_MASTER=DDR	SYNC_DATE=12/05/2008
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SIZE D	DRAWING NUMBER 051-7892	REV. A.O.O
SCALE NONE	SHT 27	OF 97







5V S3 WLAN FET

Part	TPCP8102
Type	P-Channel
Rds(on)	14 mOhm @4.5V
Loading	0.8 A (EDP)

AIRPORT

ALS
CAMERA

BLUETOOTH

Right Clutch Connector

SYNC_MASTER=MUXGFX SYNC_DATE=12/08/2008

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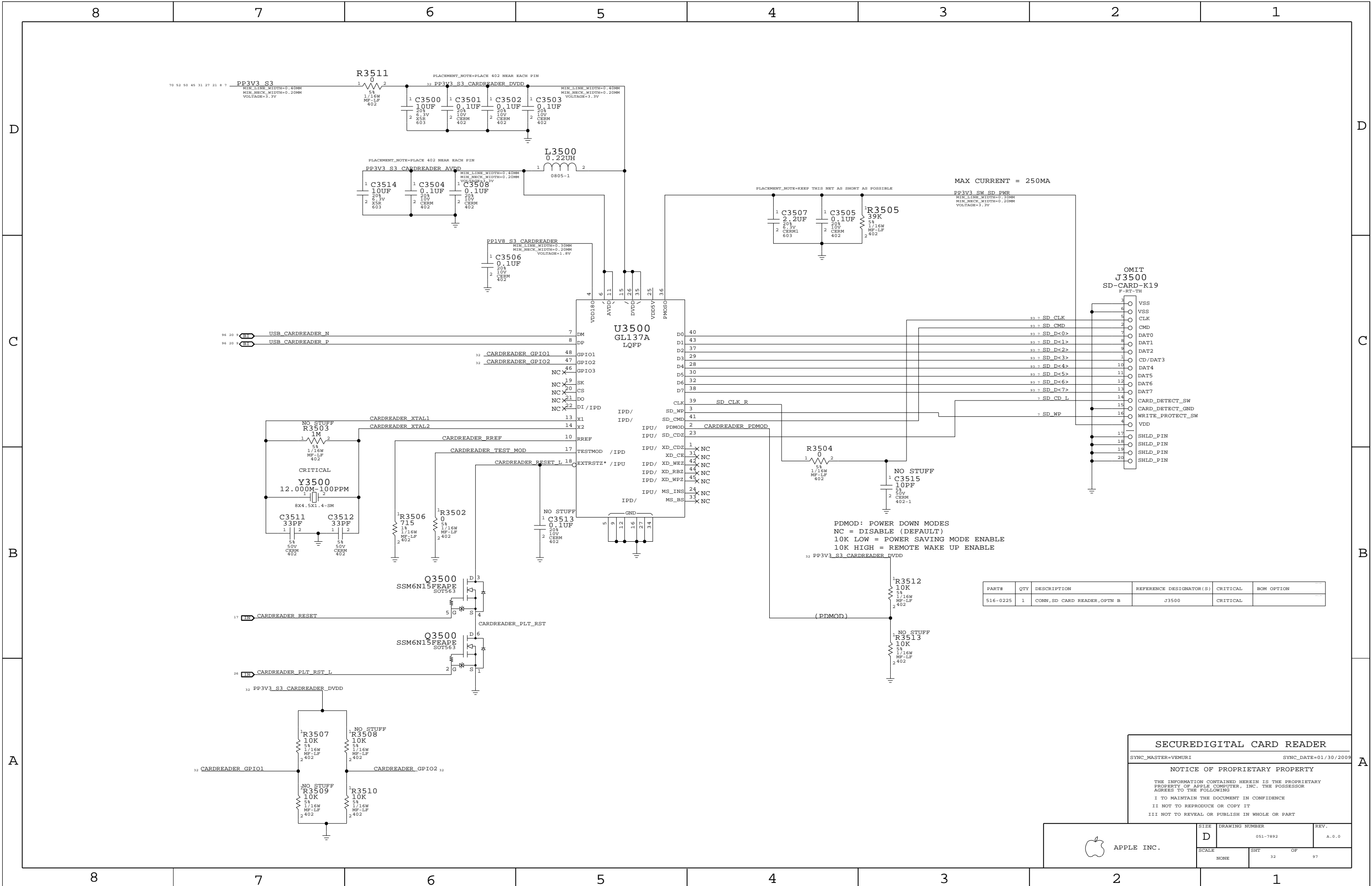
II NOT TO REPRODUCE OR COPY IT

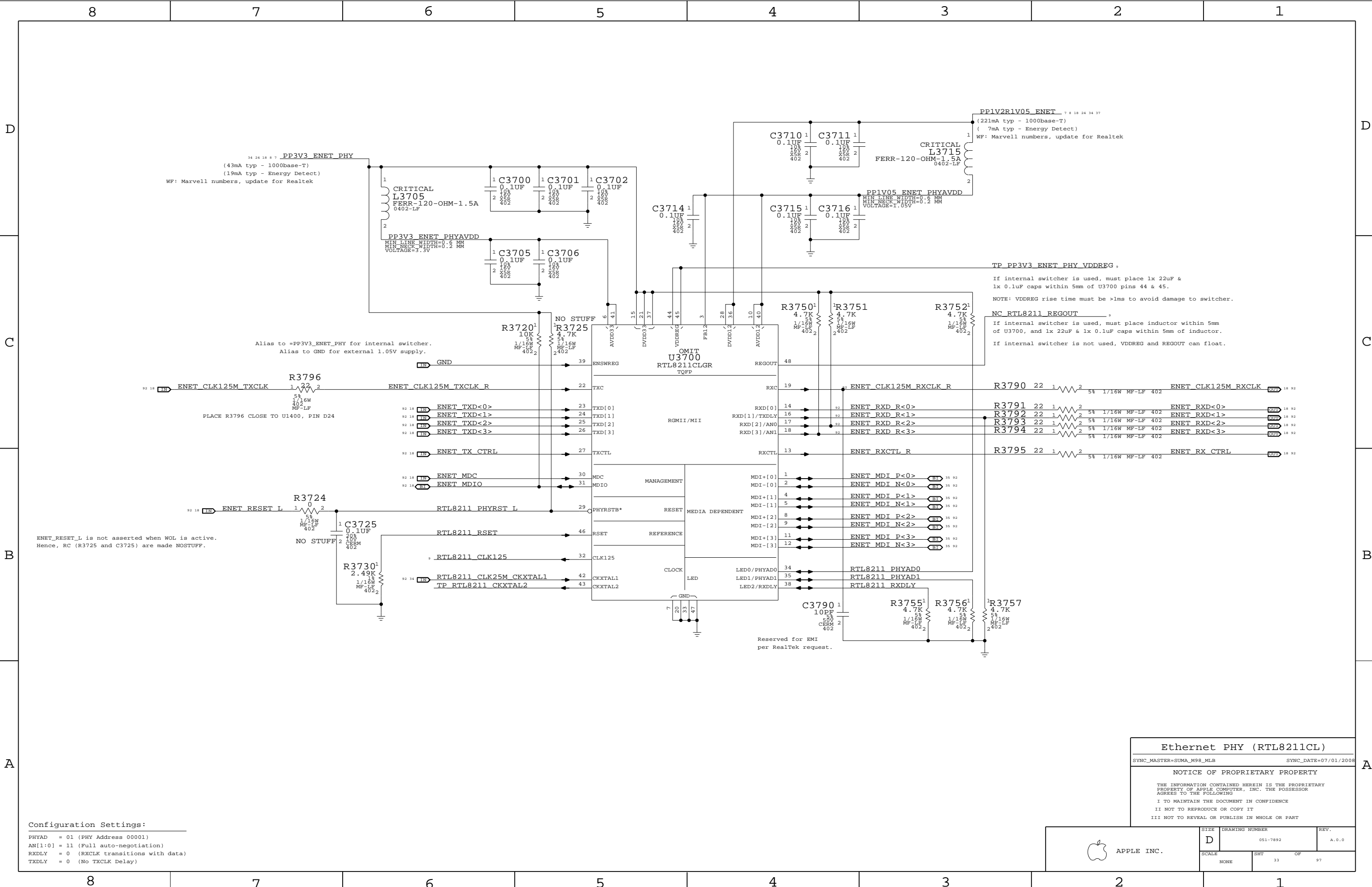
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	31	97





Configuration Settings:

PHYAD	= 01 (PHY Address 00001)
AN[1:0]	= 11 (Full auto-negotiation)
RXDLY	= 0 (RXCLK transitions with data)
TXDLY	= 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)		
SYNC_MASTER=SUMA_M98_MLB		SYNC_DATE=07/01/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7892	A.0.0
SCALE		SHT	OF
NONE		33	97

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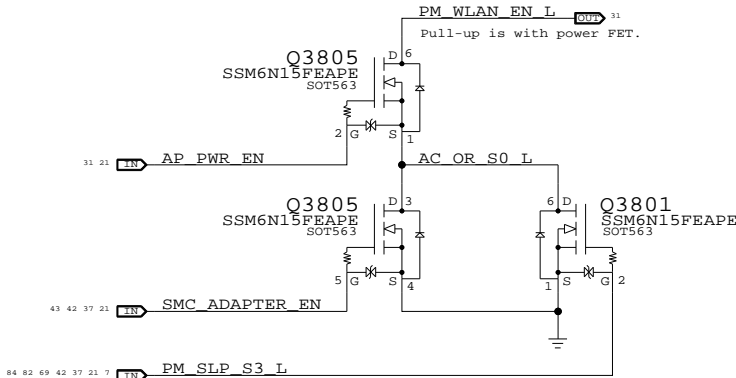
B

A

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

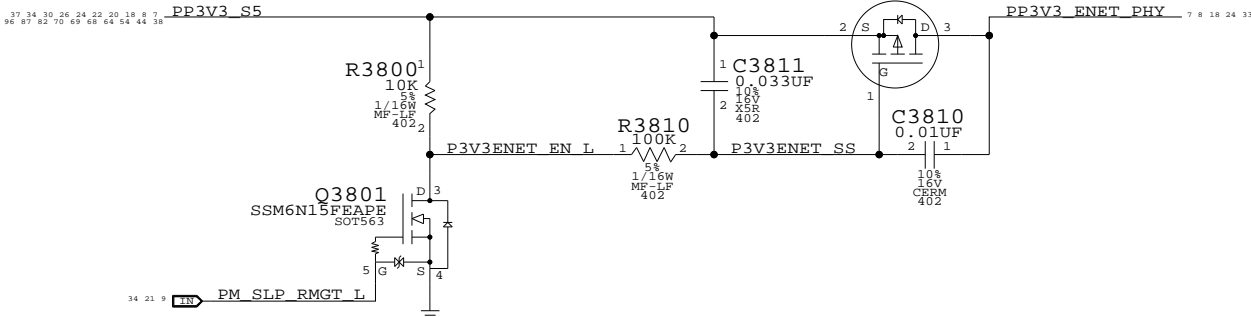
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



3.3V ENET FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

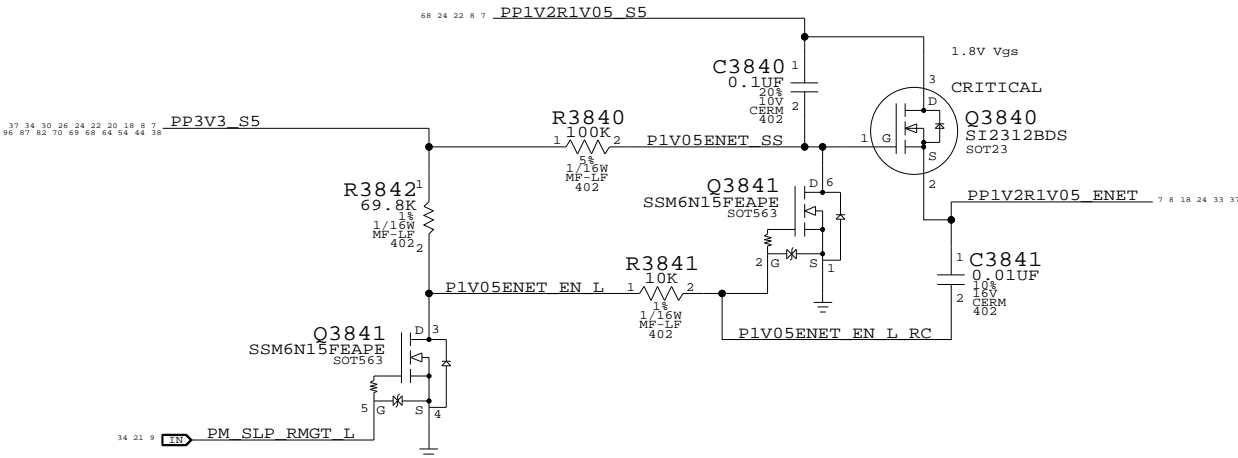
CRITICAL
Q3810
NTR4101P
SOT-23-HF



MOBILE:
Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

1.05V ENET FET

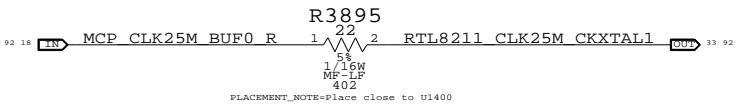
1.8V Vgs
CRITICAL
Q3840
SI2312BDS
SOT23



Non-ARB:
Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

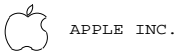


Ethernet & AirPort Support

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

NOTICE OF PROPRIETARY PROPERTY

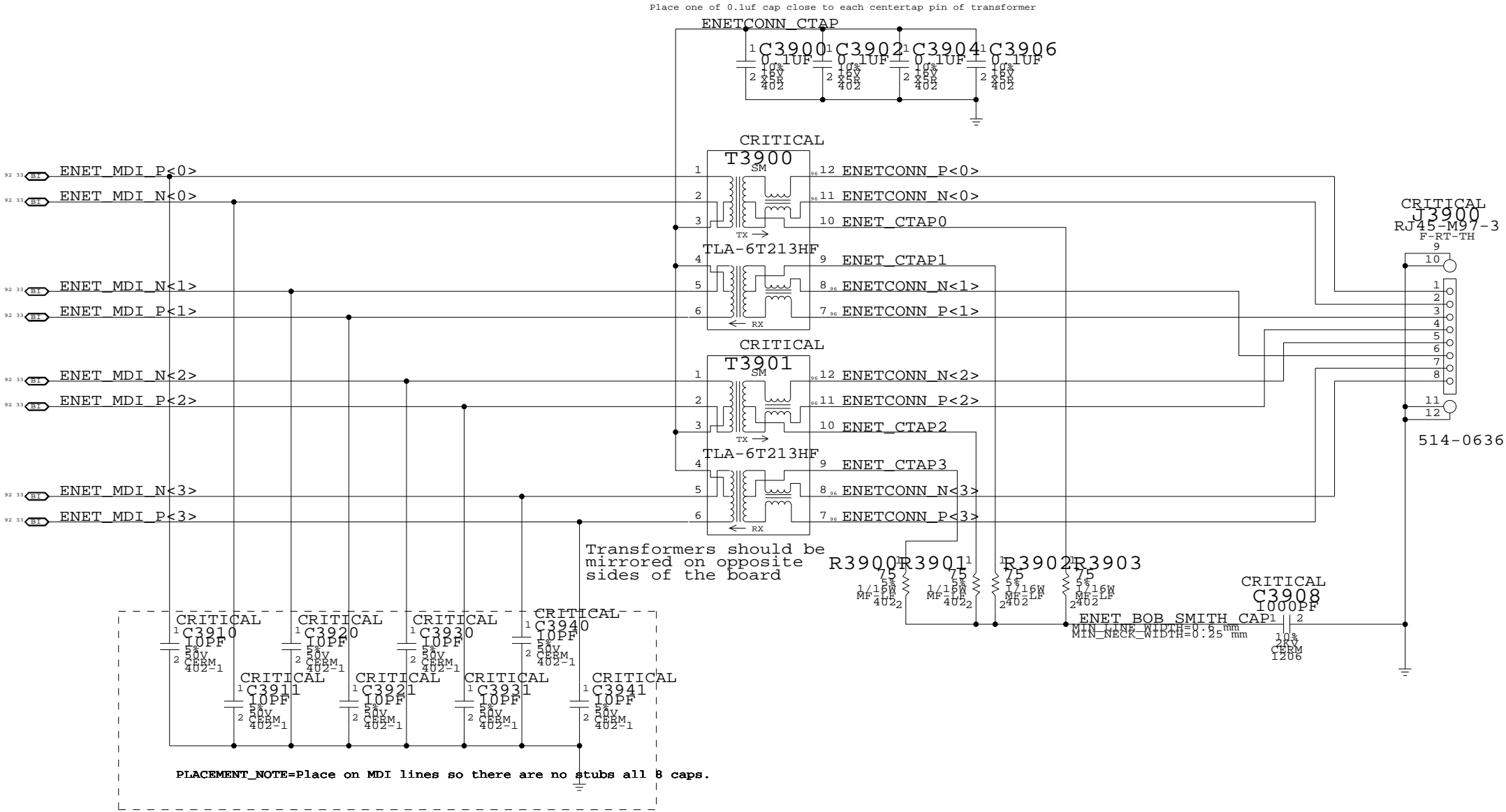
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SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	34	97

Page Notes

Power aliases required by this page:
(NONE)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)

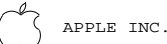


Ethernet Connector

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=12/16/2008

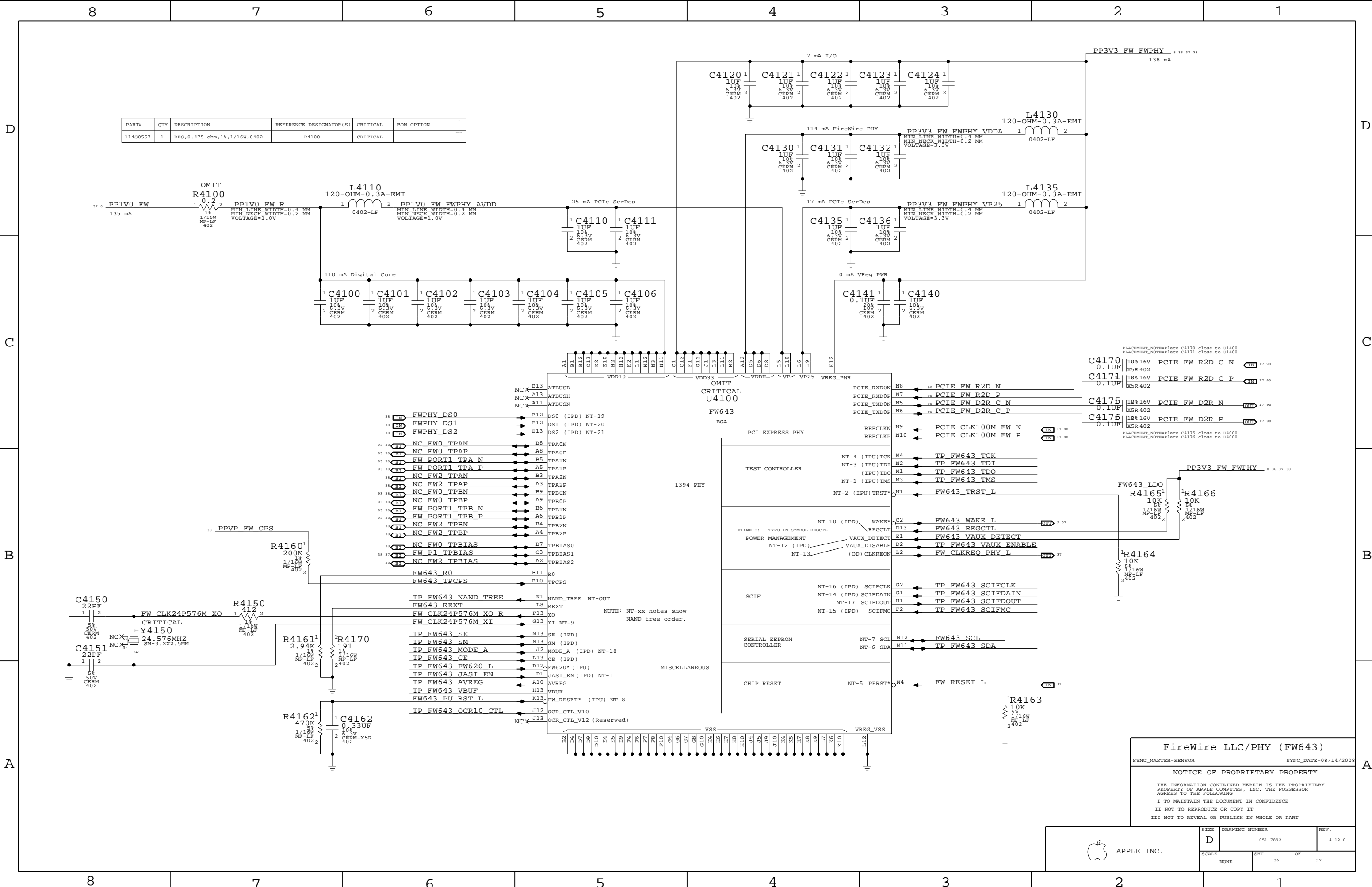
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APPLE INC.

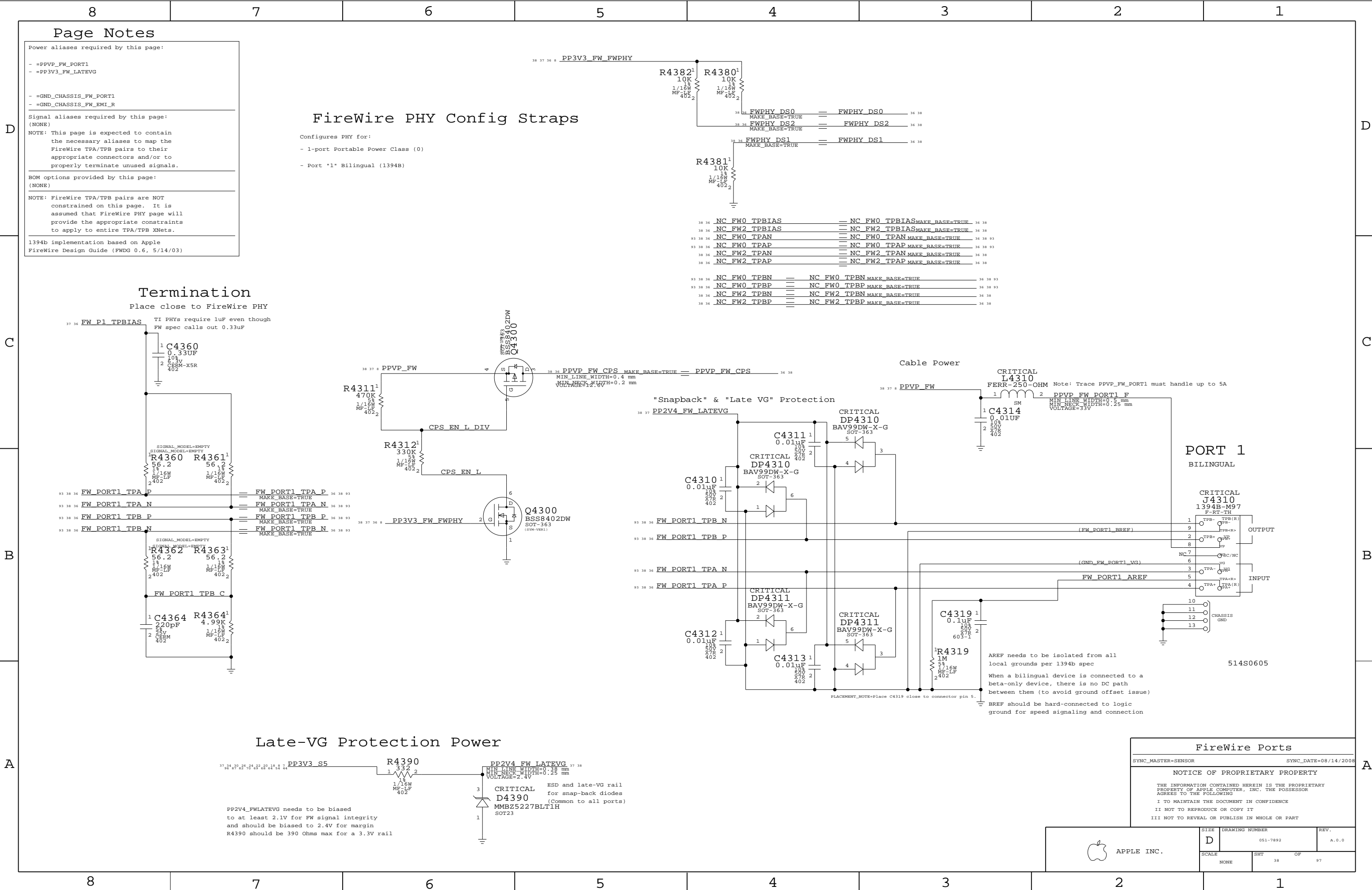
SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	35	97

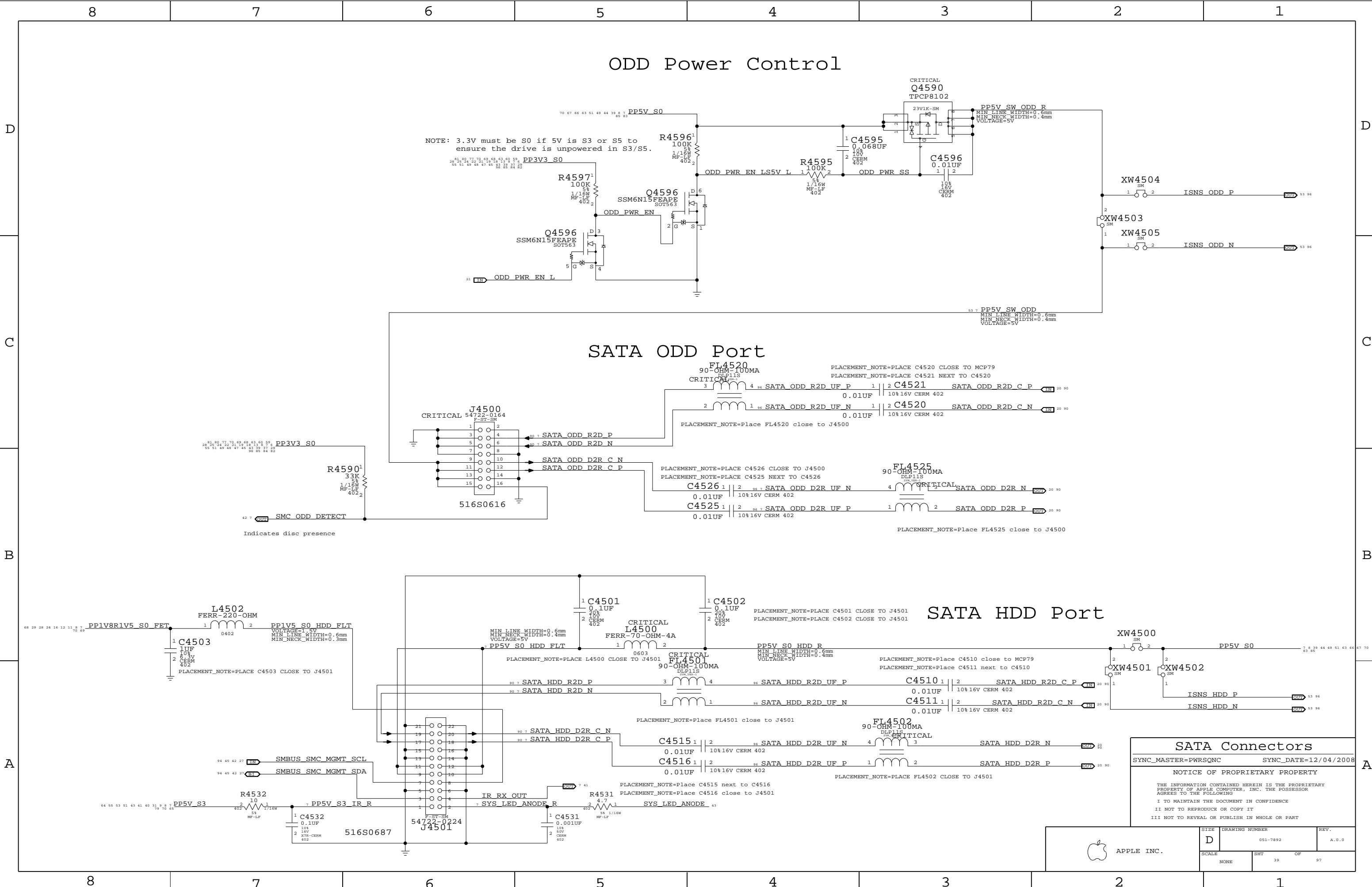


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11480557	1	RES,0.475 ohm,1%,1/16W,0402	R4100	CRITICAL	

FireWire LLC/PHY (FW643)		
SYNC_MASTER=SENSOR		SYNC_DATE=08/14/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7892	4.12.0
SCALE		SHT	OF
NONE		36	97





ODD Power Control

SATA ODD Port

SATA HDD Port

SATA Connectors

SYNC_MASTER=PWRSQNC SYNC_DATE=12/04/2008

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APPLE INC.

SIZE D DRAWING NUMBER 051-7892 REV. A.0.0

SCALE NONE SHT 39 OF 97

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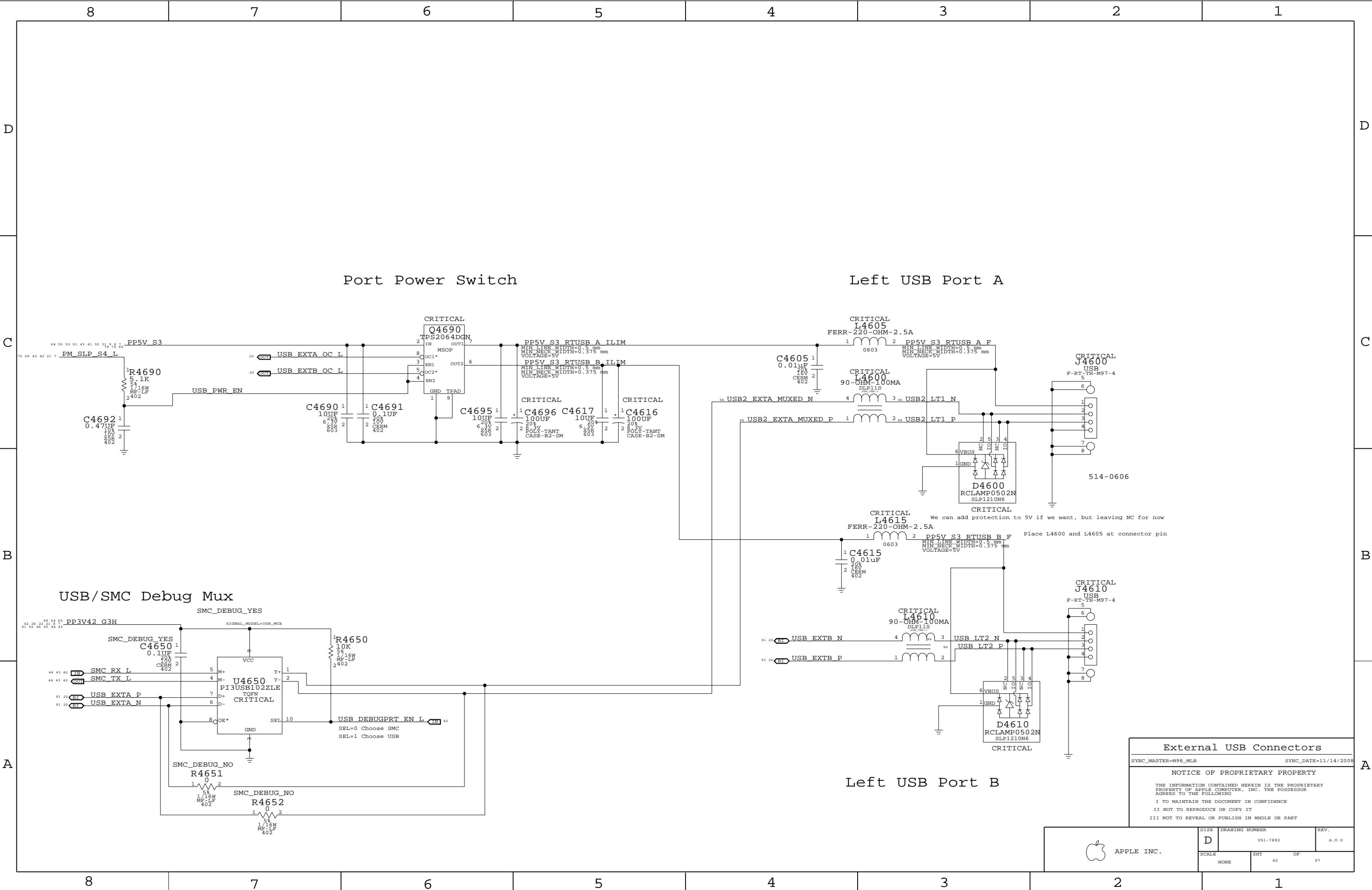
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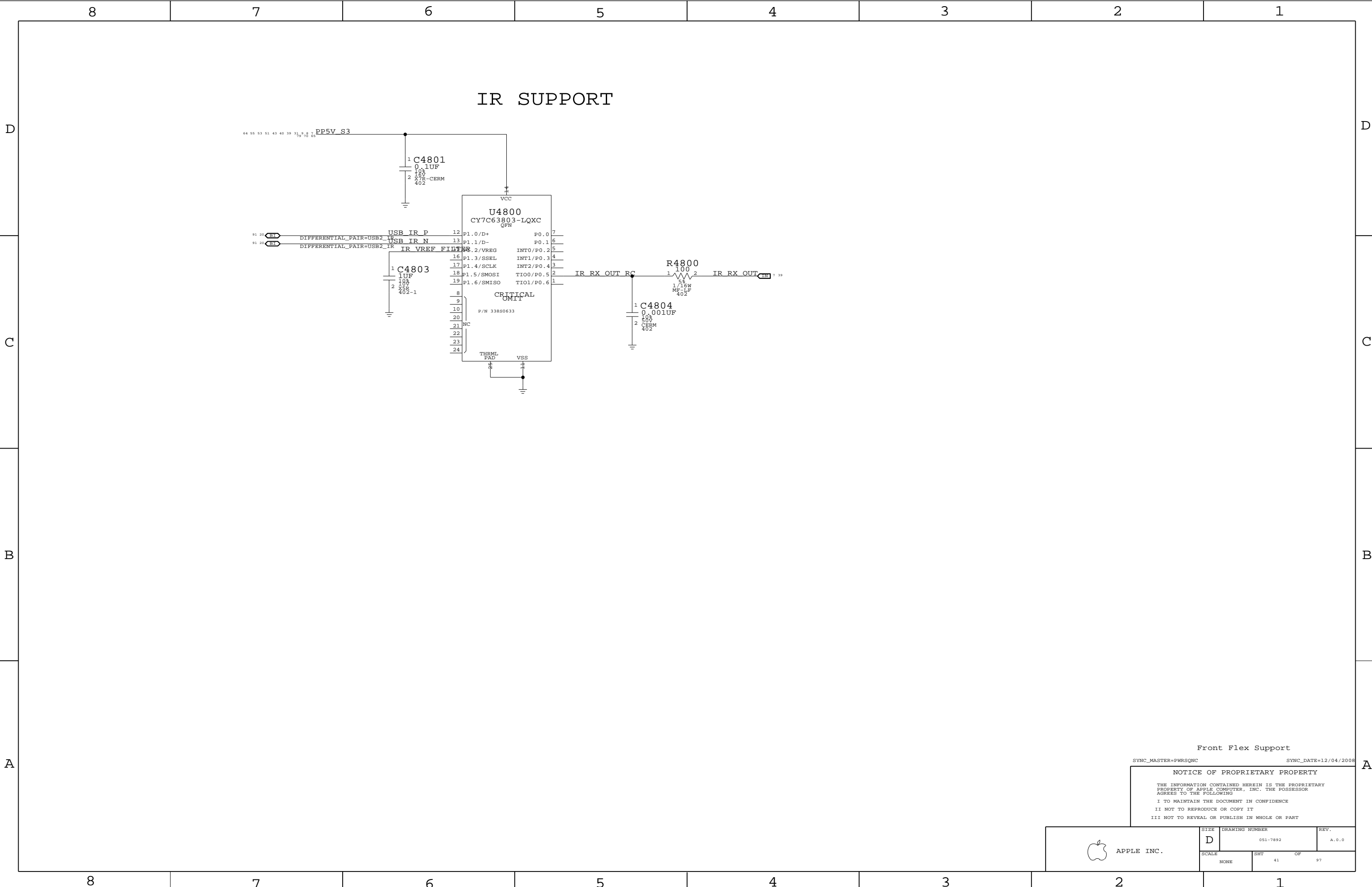
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External USB Connectors		
SYNC_MASTER=M98_MLB		SYNC_DATE=11/14/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7892	A.0.0
SCALE		SHT	OF
NONE		40	97



Front Flex Support

SYNC_MASTER=PWRSONC SYNC_DATE=12/04/2008

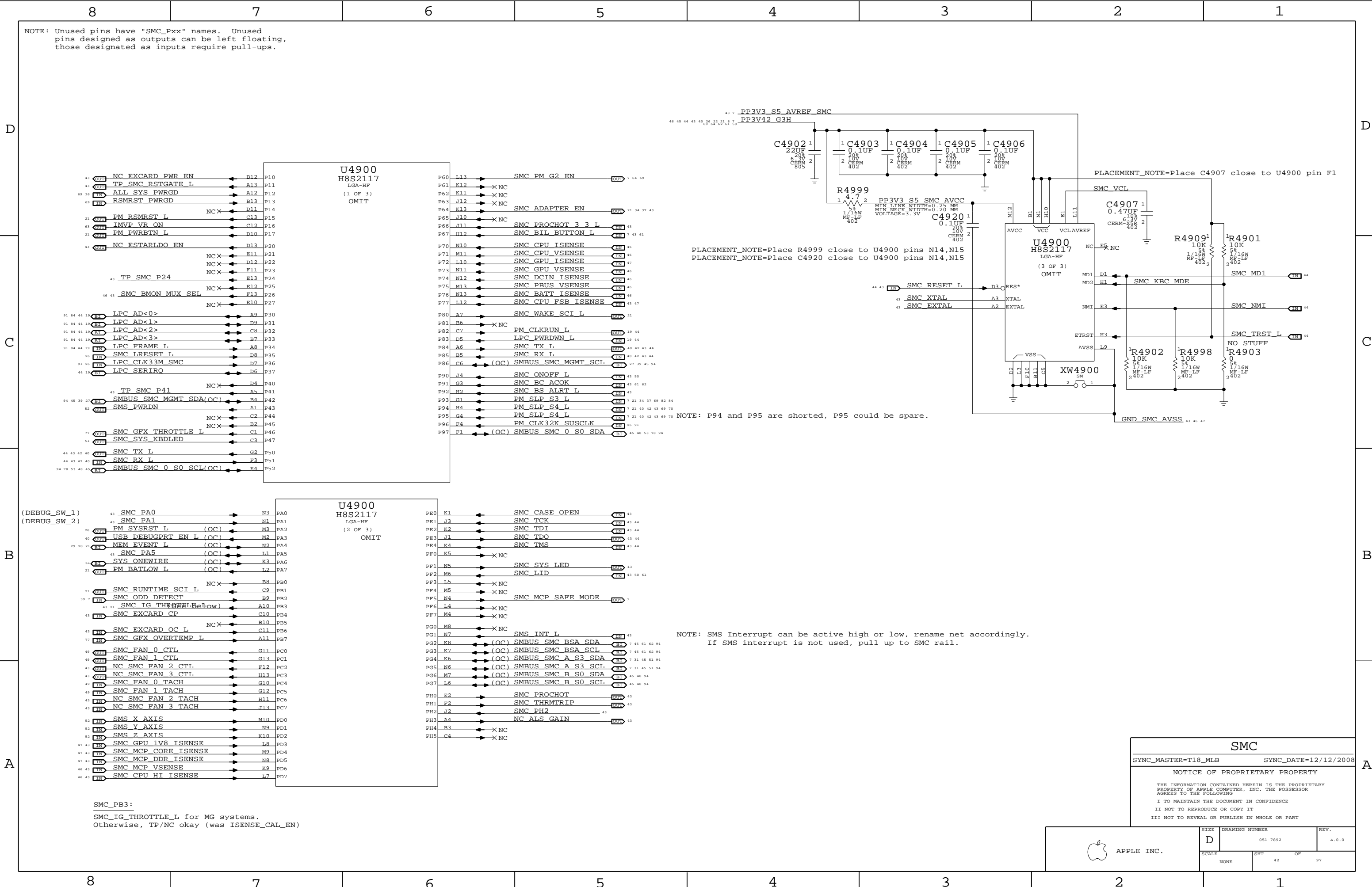
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	41	97



NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

D

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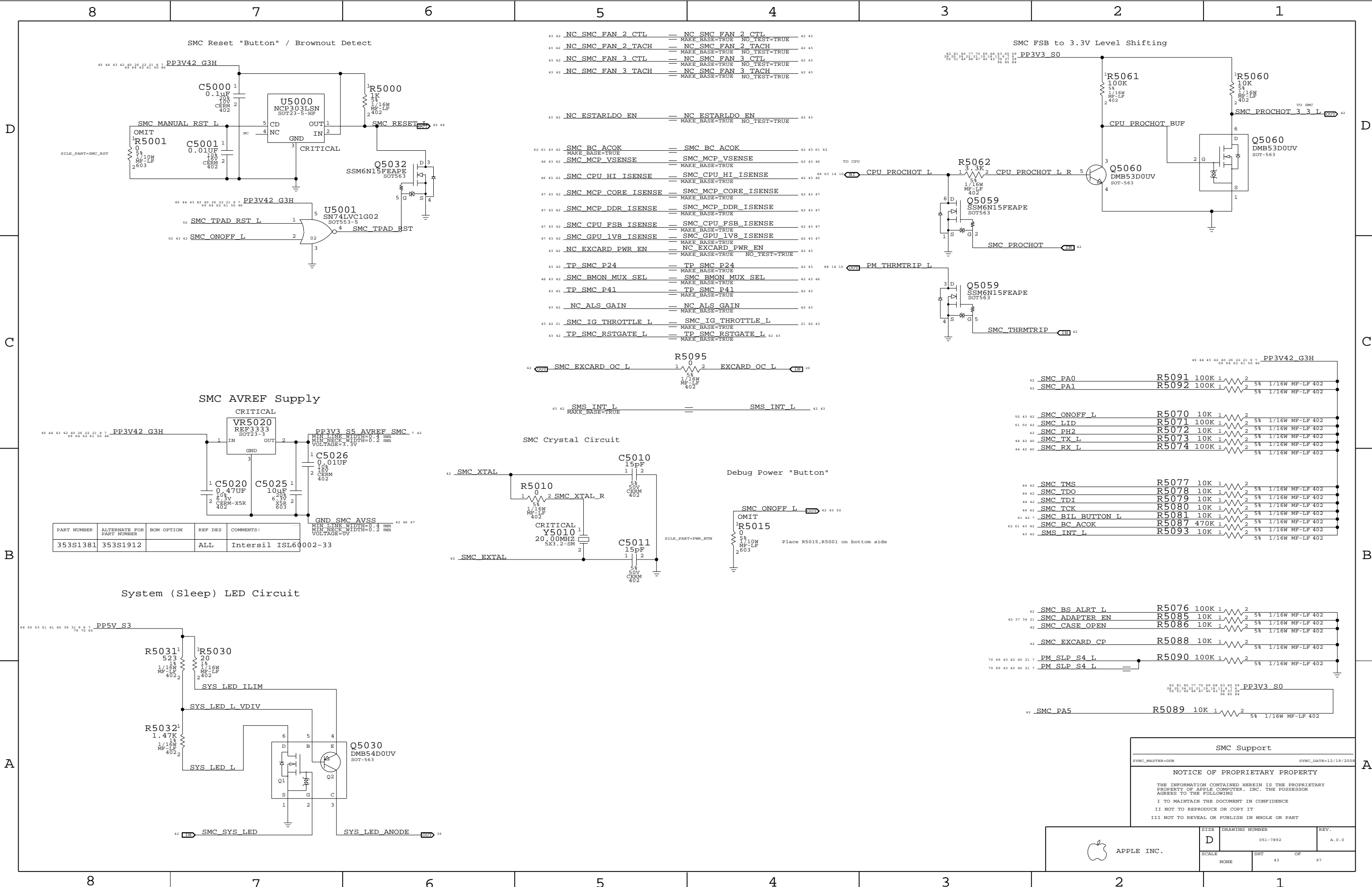
A

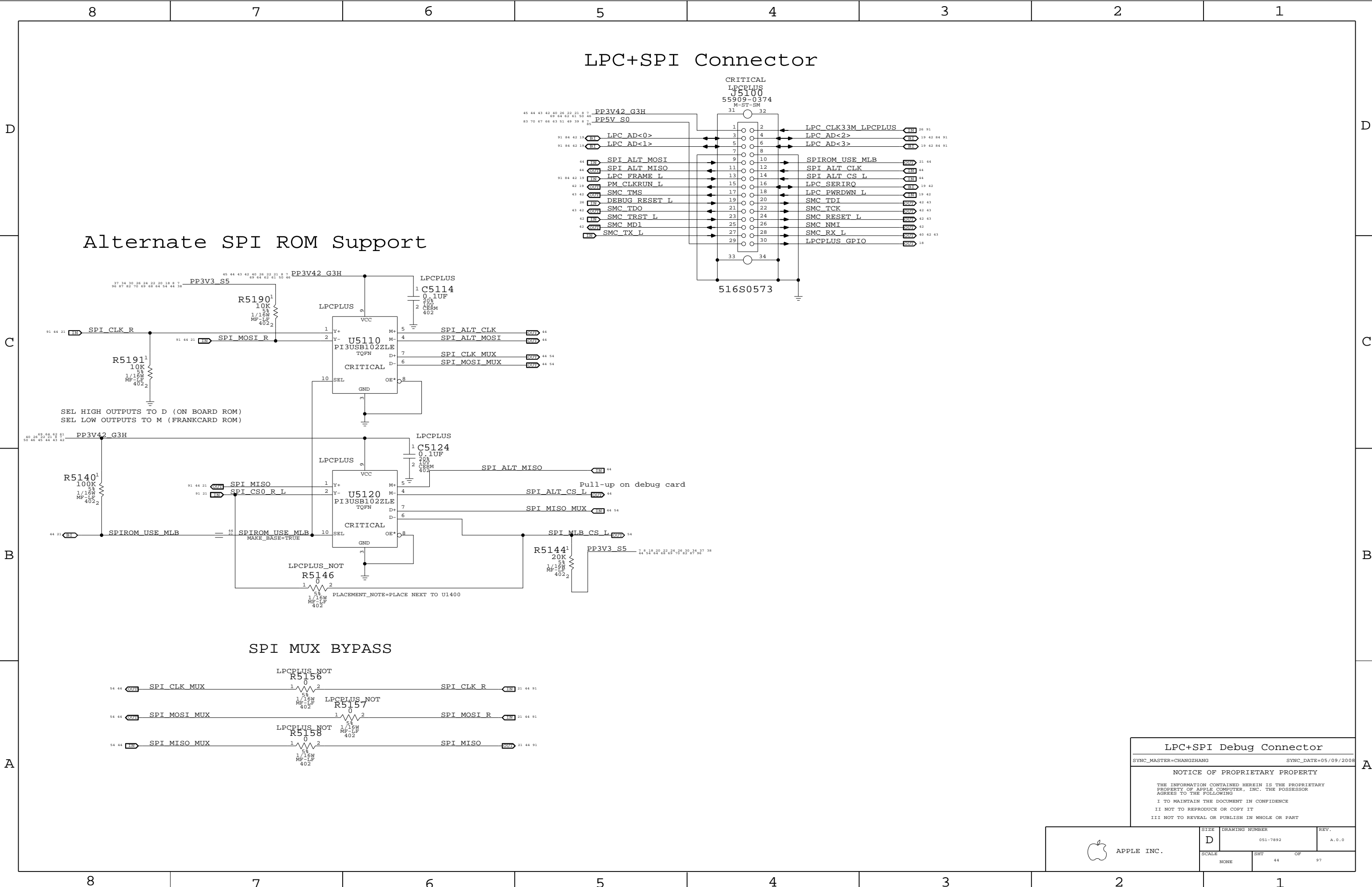
D

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LPC+SPI Connector

Alternate SPI ROM Support

SPI MUX BYPASS

LPC+SPI Debug Connector

SYNC_MASTER=CHANGZHANG

SYNC_DATE=05/09/2008

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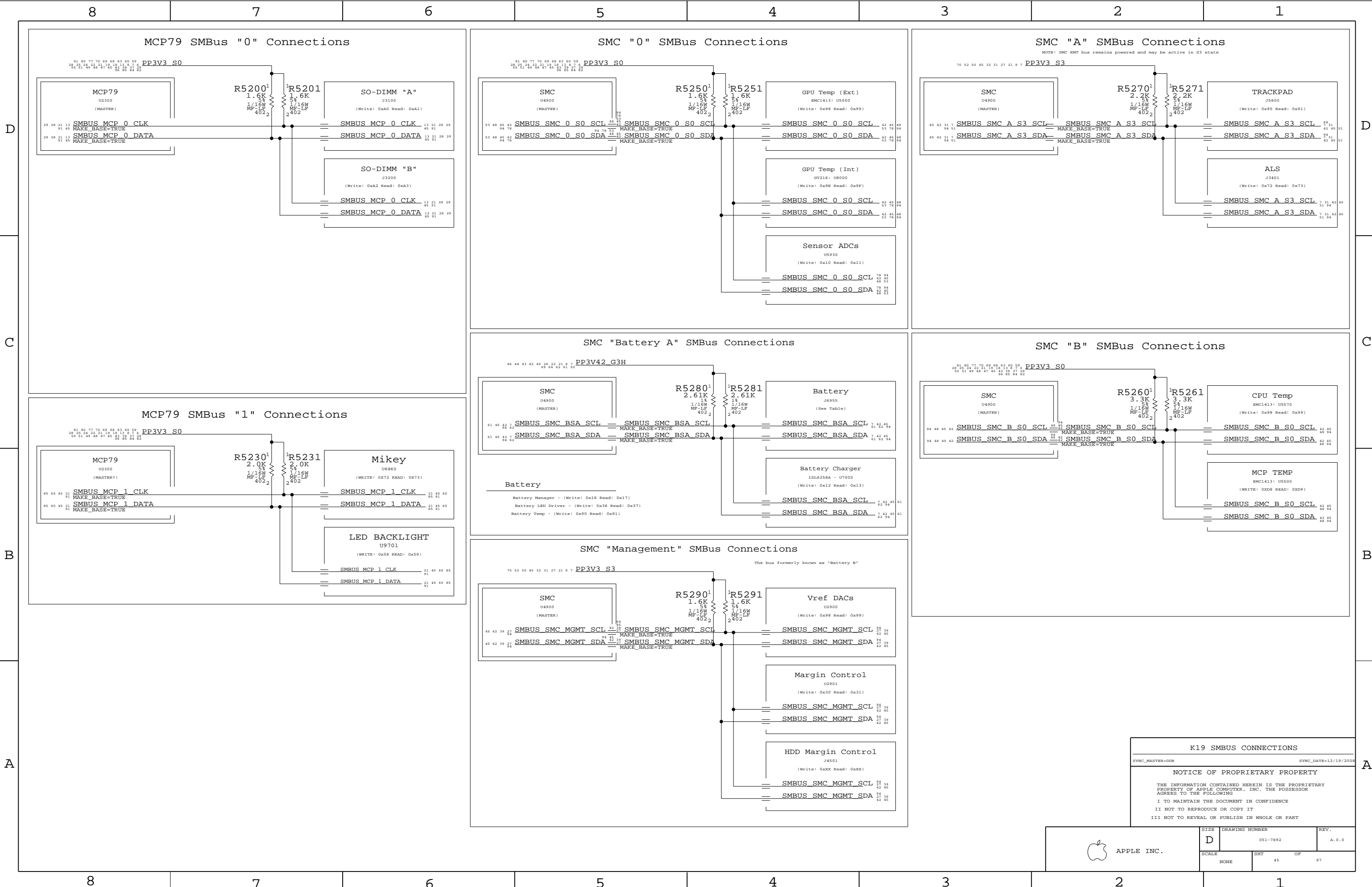
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	44	97



K19 SMBUS CONNECTIONS

SYNC_MASTER=DOR

SYNC_DATE=12/19/2008

NOTICE OF PROPRIETARY PROPERTY

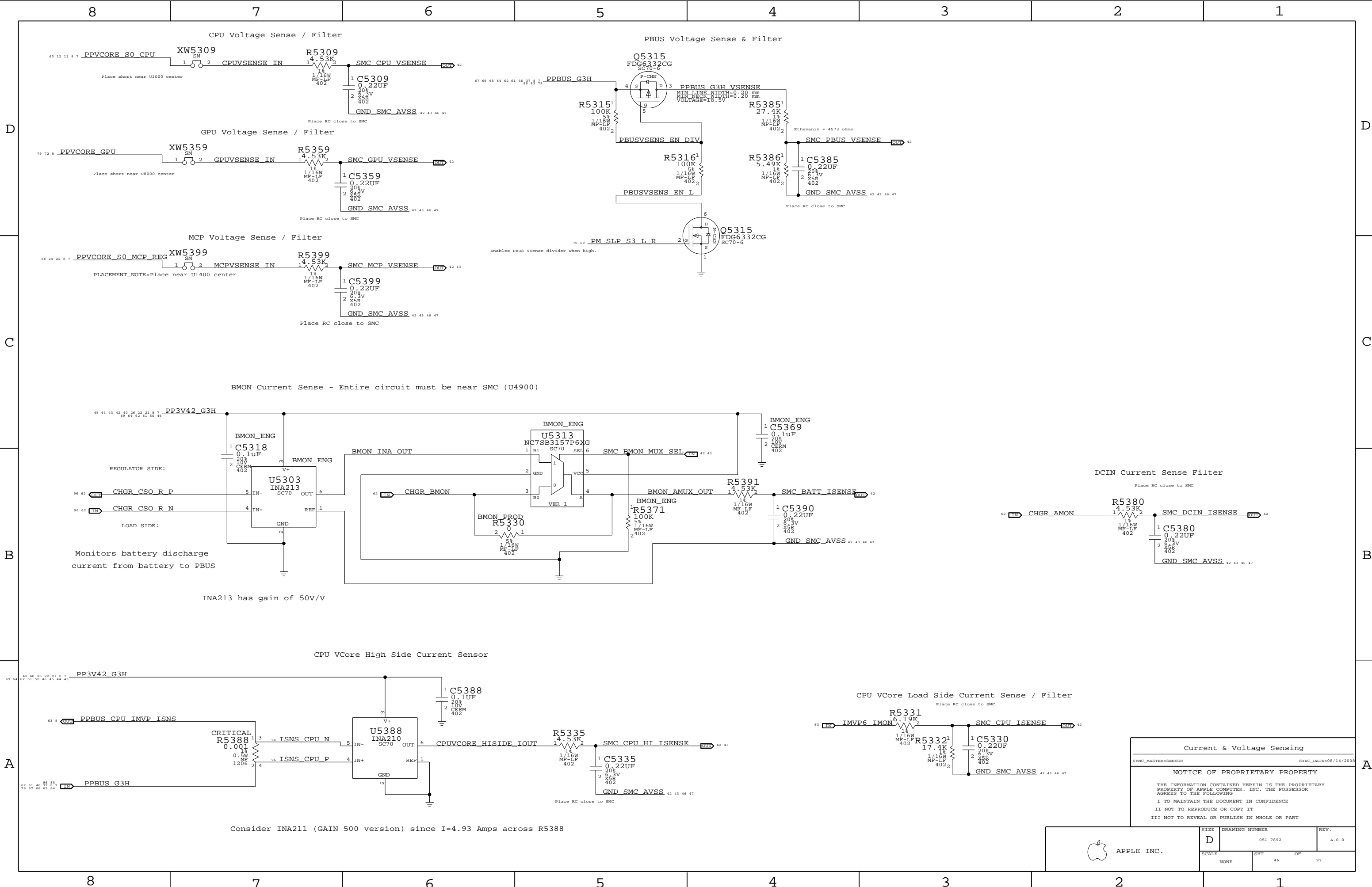
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7892	A.0.0
SCALE		SHT	OF
NONE		45	97

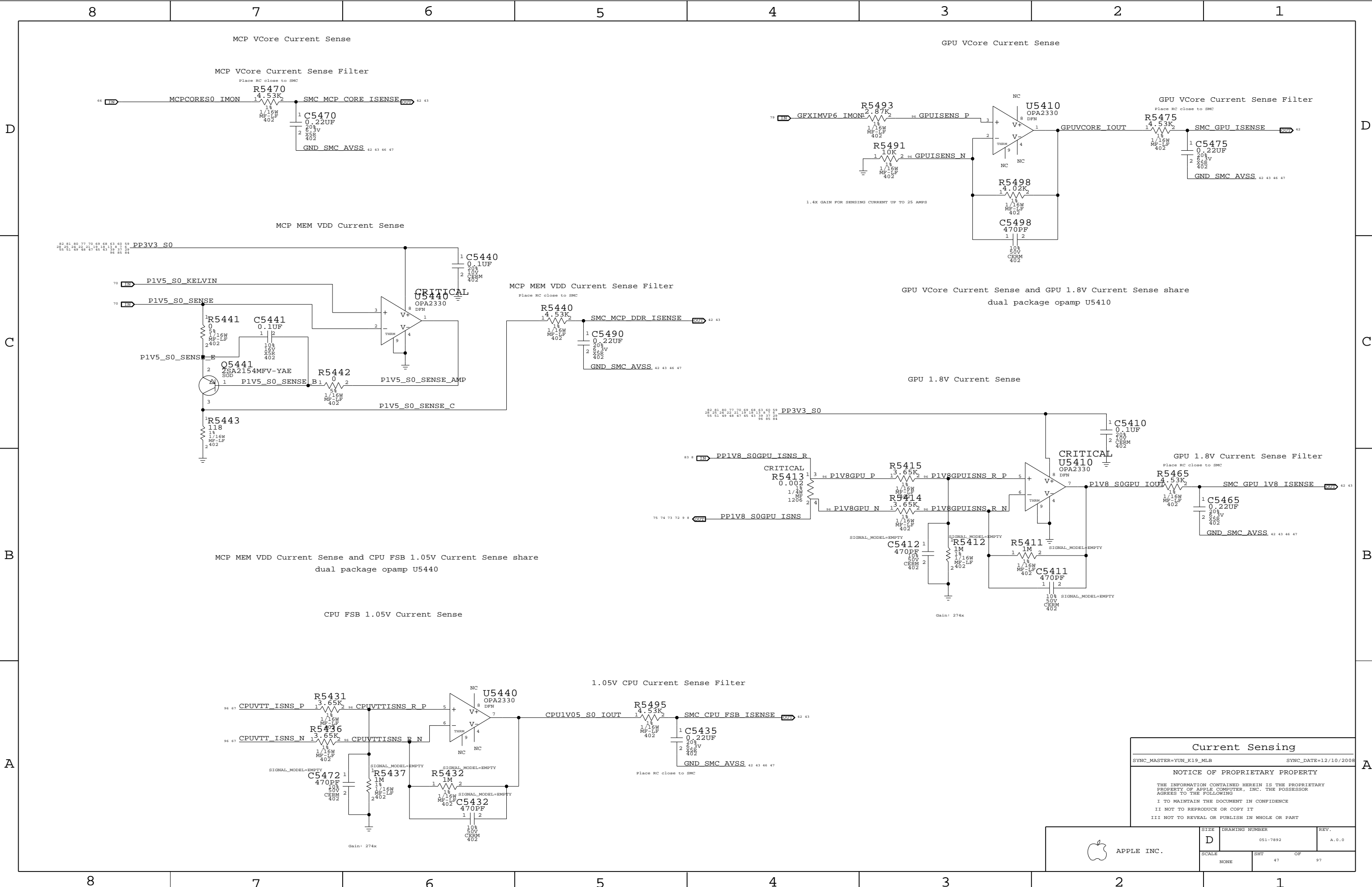


Current & Voltage Sensing		
SYNC_MASTER=SENSOR		SYNC_DATE=08/14/2008
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SCALE NONE	SHT 46	OF 97



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0



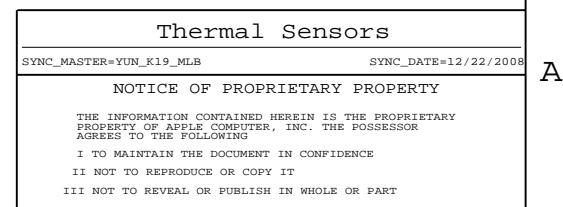
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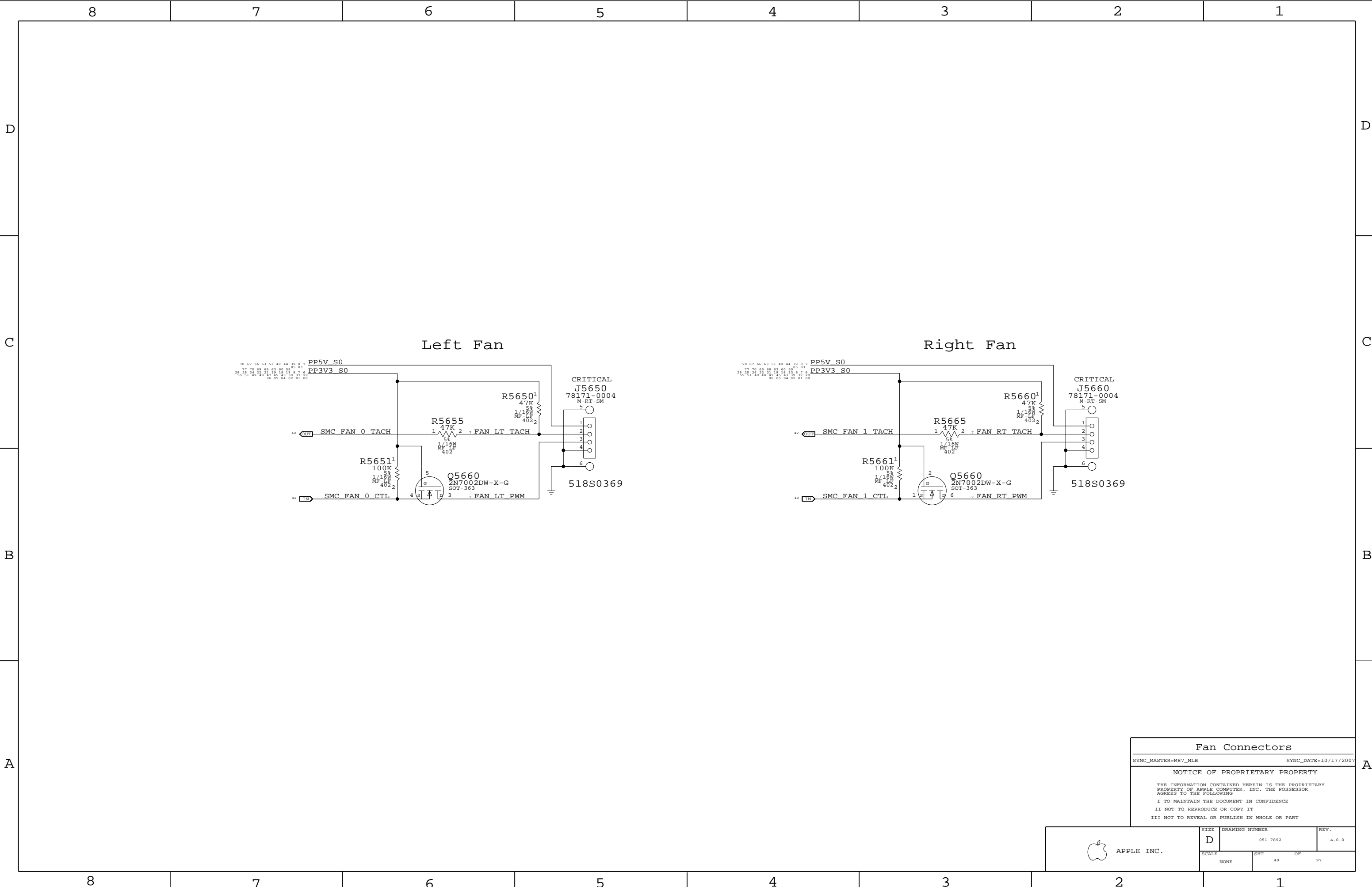


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Fan Connectors

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

NOTICE OF PROPRIETARY PROPERTY

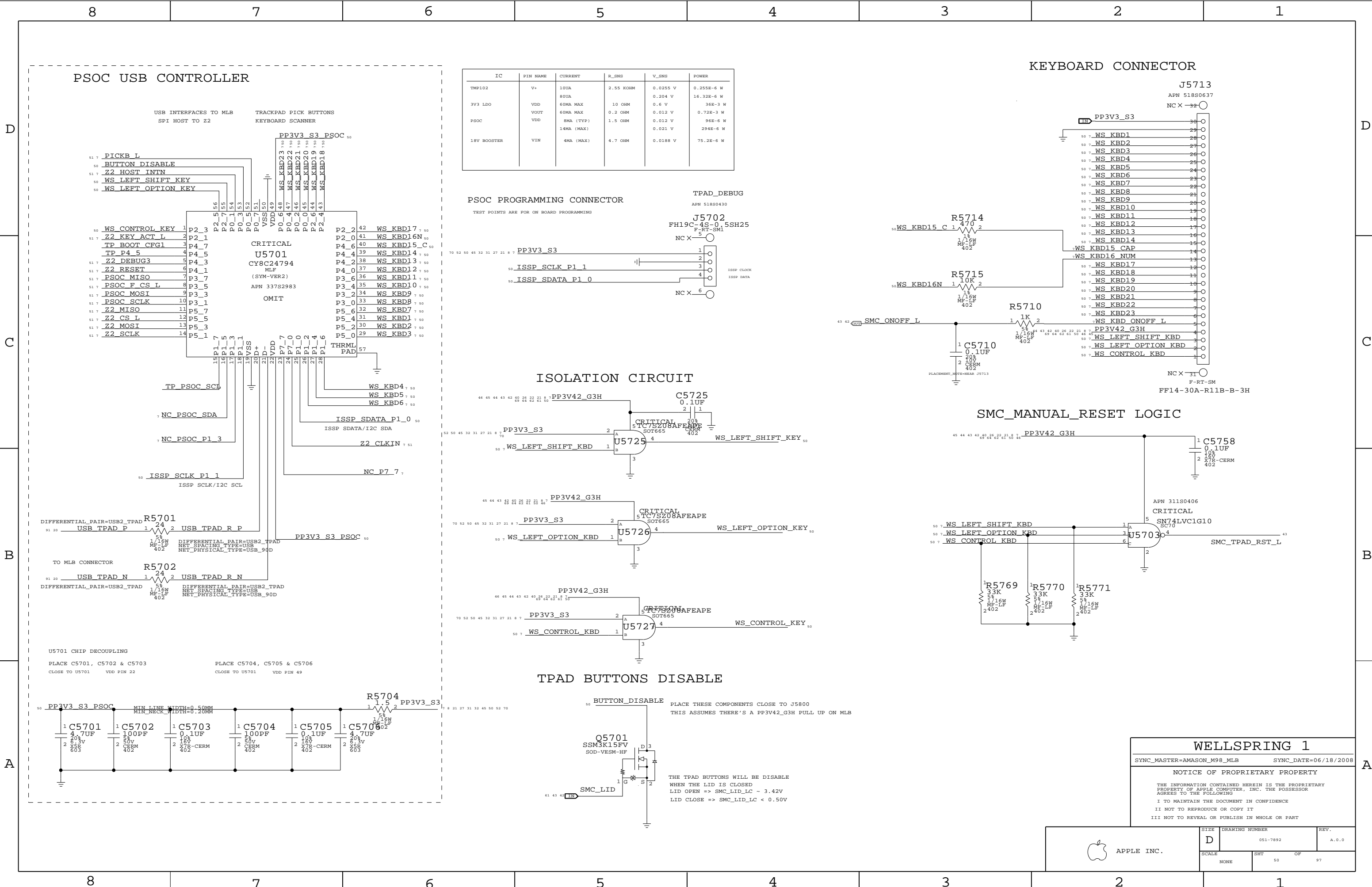
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7892	A.0.0
SCALE		SHT	OF
NONE		49	97



IC	PIN NAME	CURRENT	R _{SMS}	V _{SMS}	POWER
TMP102	V+	100A	2.55 KOHM	0.0255 V	0.255E-6 W
3V3 LDO	VDD	800A	10 OHM	0.204 V	16.32E-6 W
PSOC	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
	VDD	8MA (TVP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

PSOC PROGRAMMING CONNECTOR

TEST POINTS ARE FOR ON BOARD PROGRAMMING

TPAD_DEBUG

APN 518S0430

ISOLATION CIRCUIT

TPAD BUTTONS DISABLE

KEYBOARD CONNECTOR

SMC_MANUAL_RESET_LOGIC

WELLSPRING 1

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=06/18/2008

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APPLE INC.

SIZE

DRAWING NUMBER

REV.

D

051-7892

A.0.0

SCALE

SHT

OF

97

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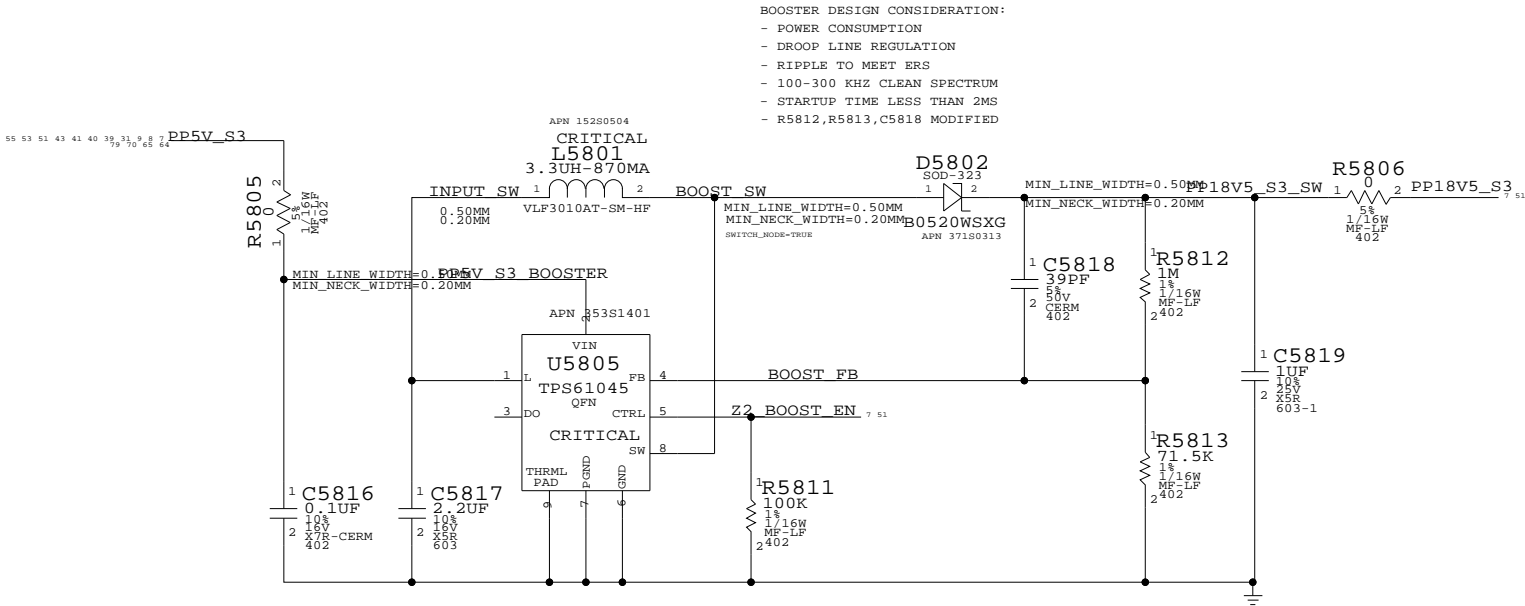
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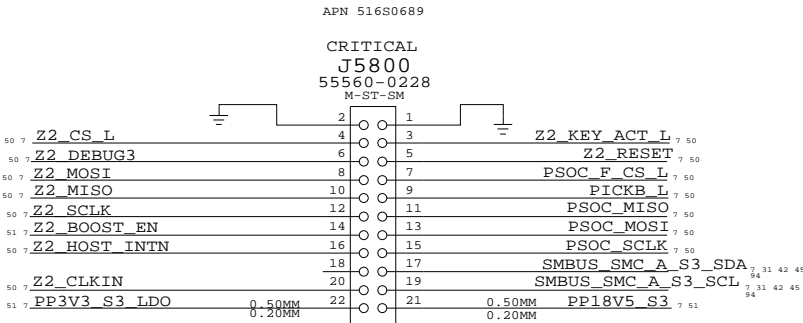
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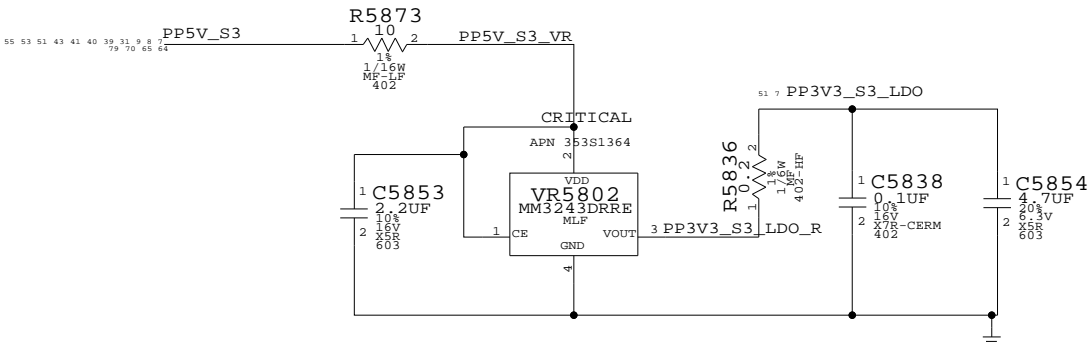
BOOSTER +18.5VDC FOR SENSORS



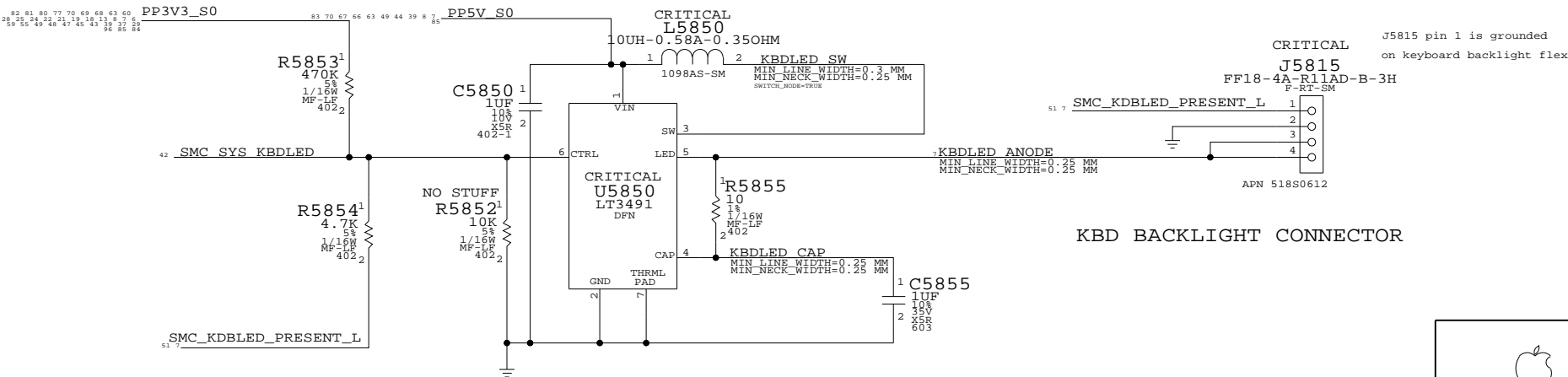
IPD FLEX CONNECTOR



3V3 LDO FOR IPD



Keyboard LED Driver



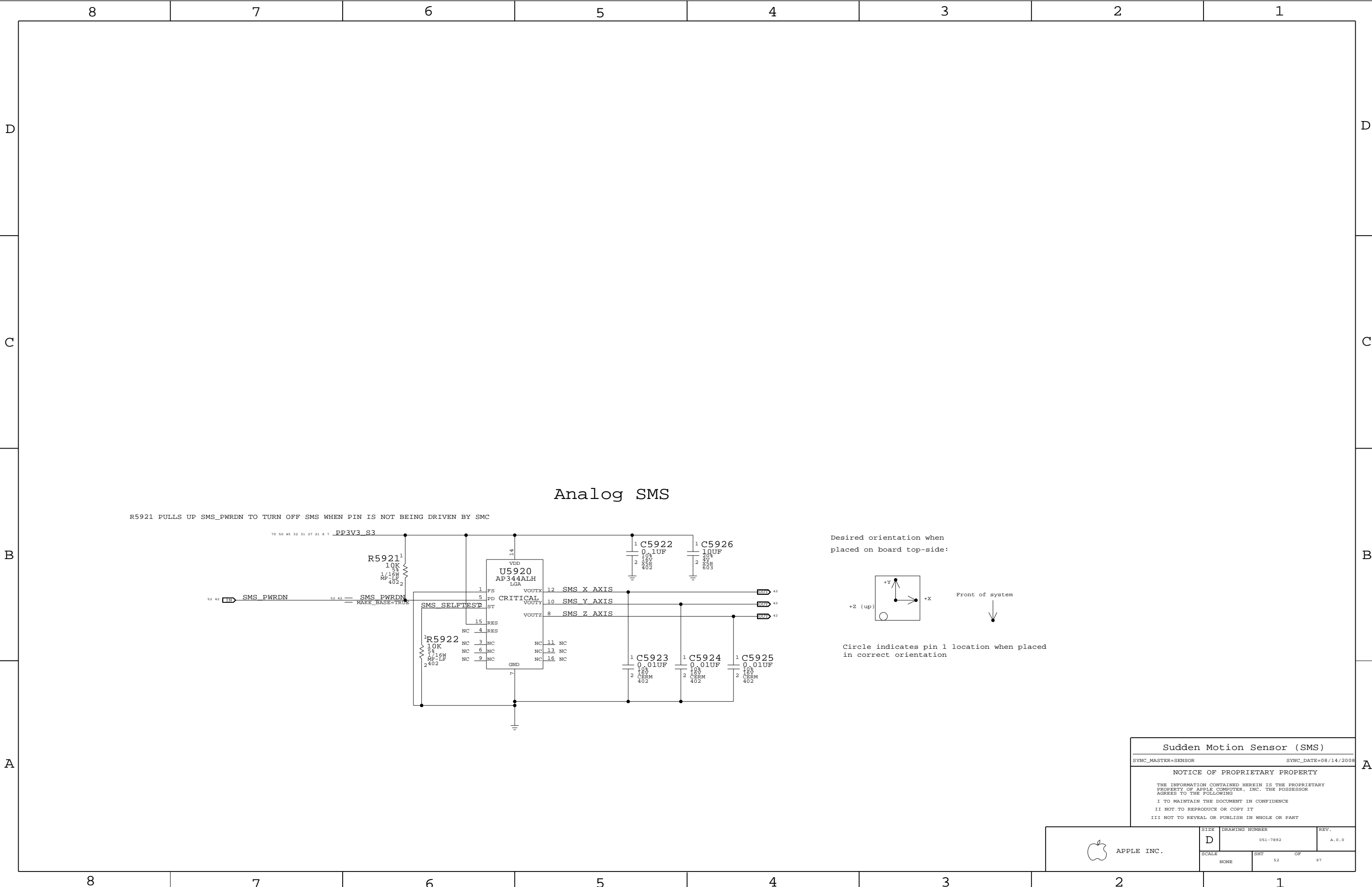
KBD BACKLIGHT CONNECTOR

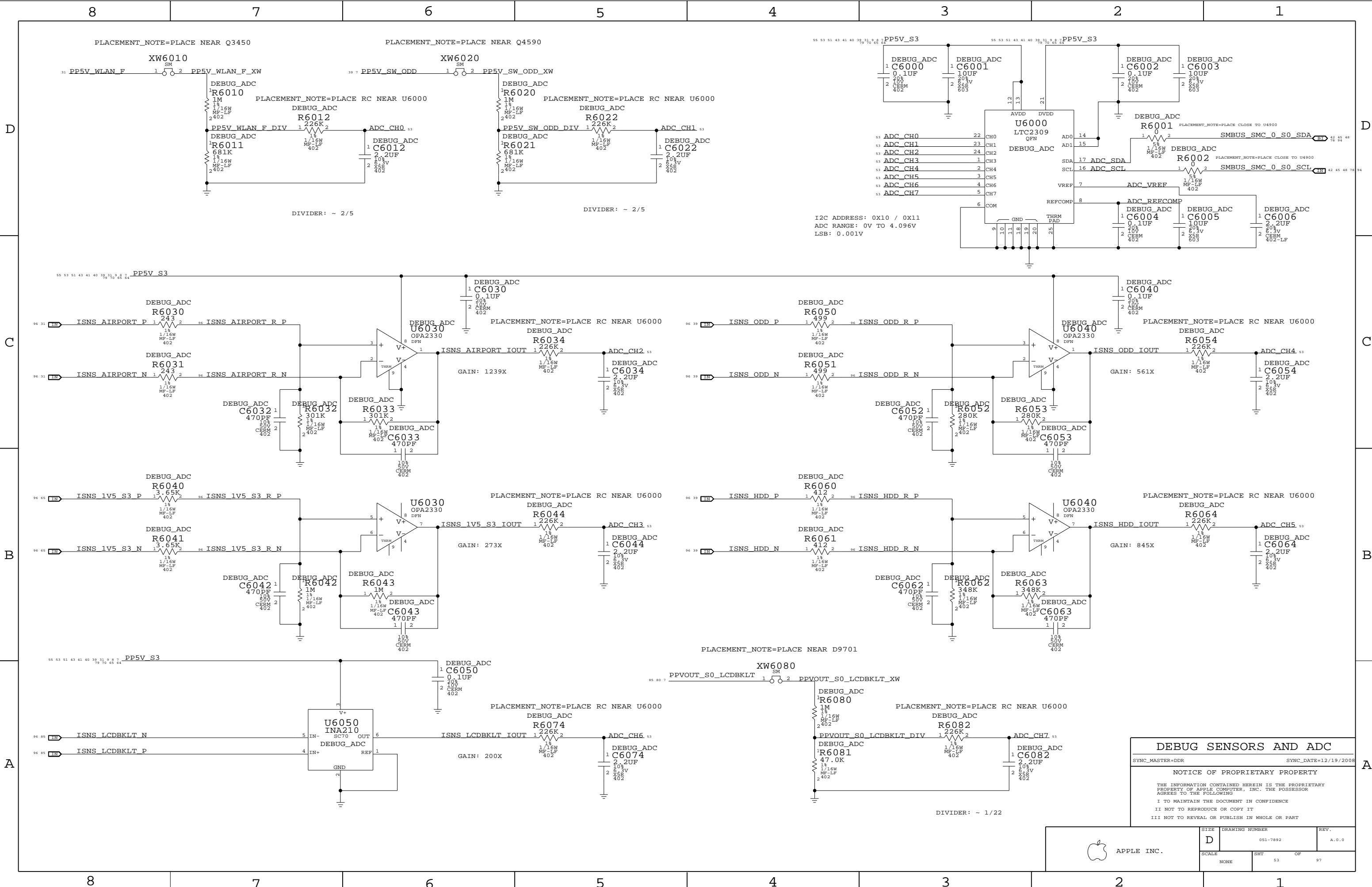
WELLSPRING 2	
SYNC_MASTER=PWRSQNC	SYNC_DATE=01/05/2009
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	51	97





D

C

B

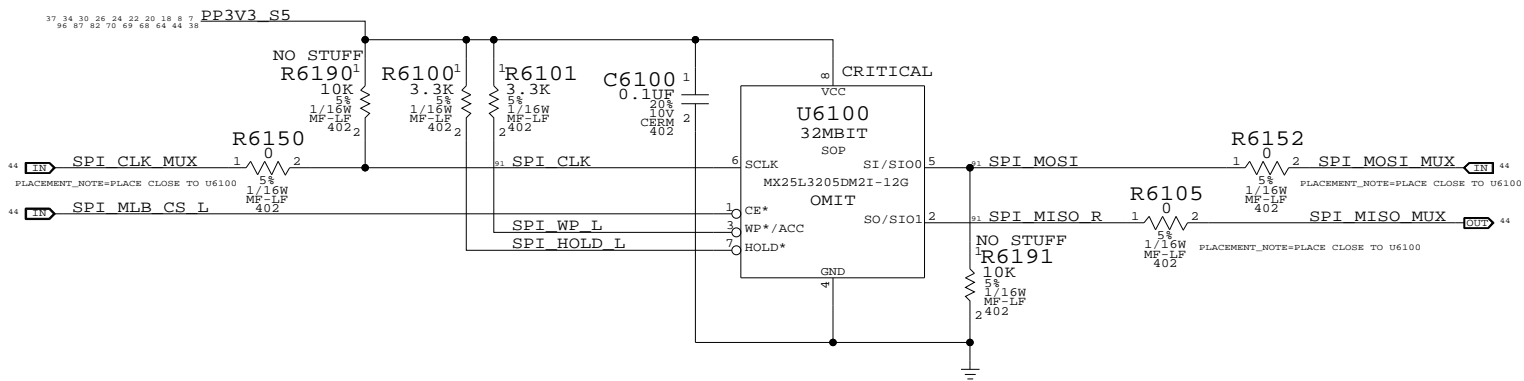
A

D

C

B

A



MCP79 SPI Frequency Select		
Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

SPI ROM

SYNC_MASTER=CHANG_M98_MLBSYNC_DATE=07/01/2008

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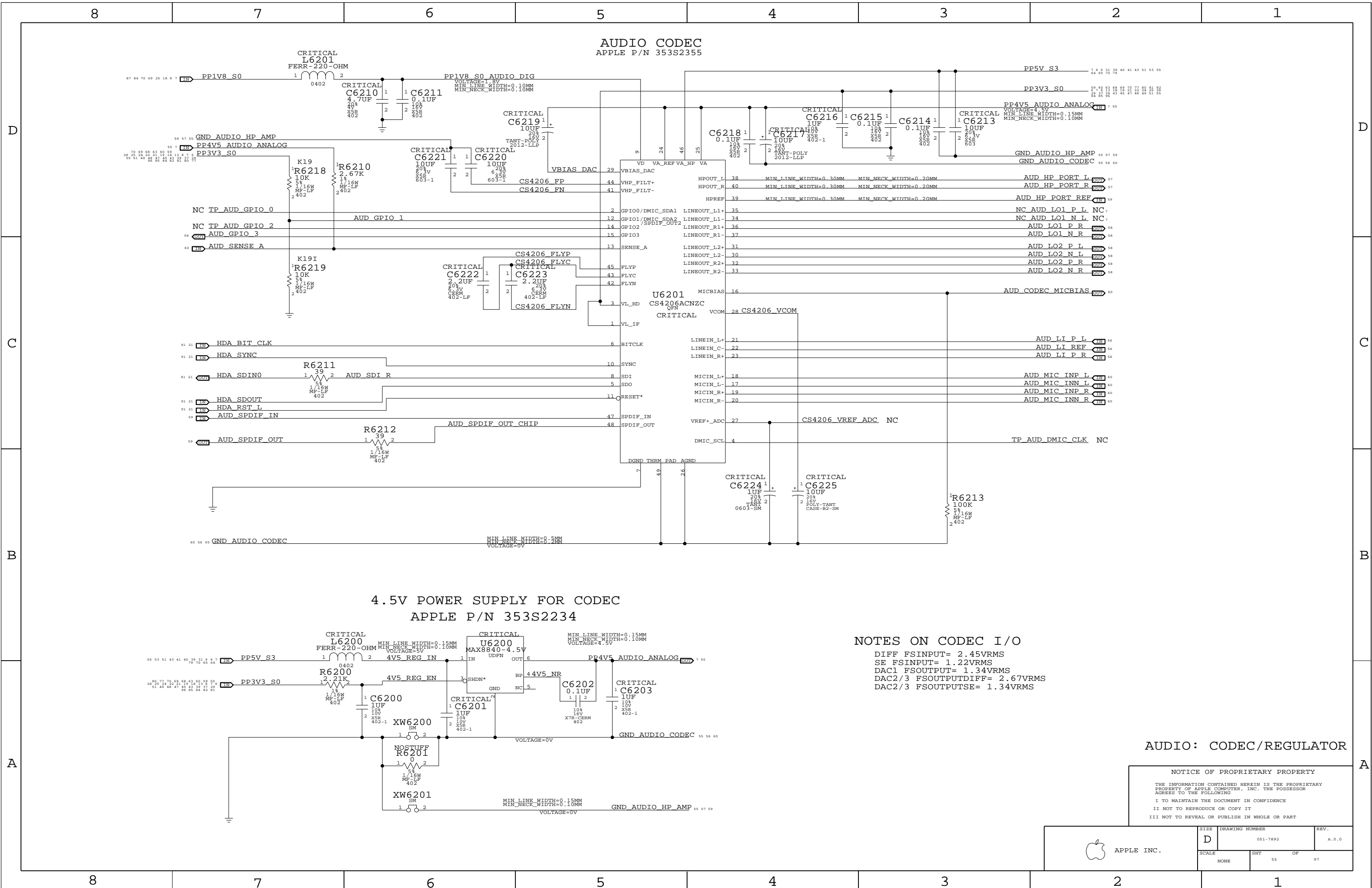
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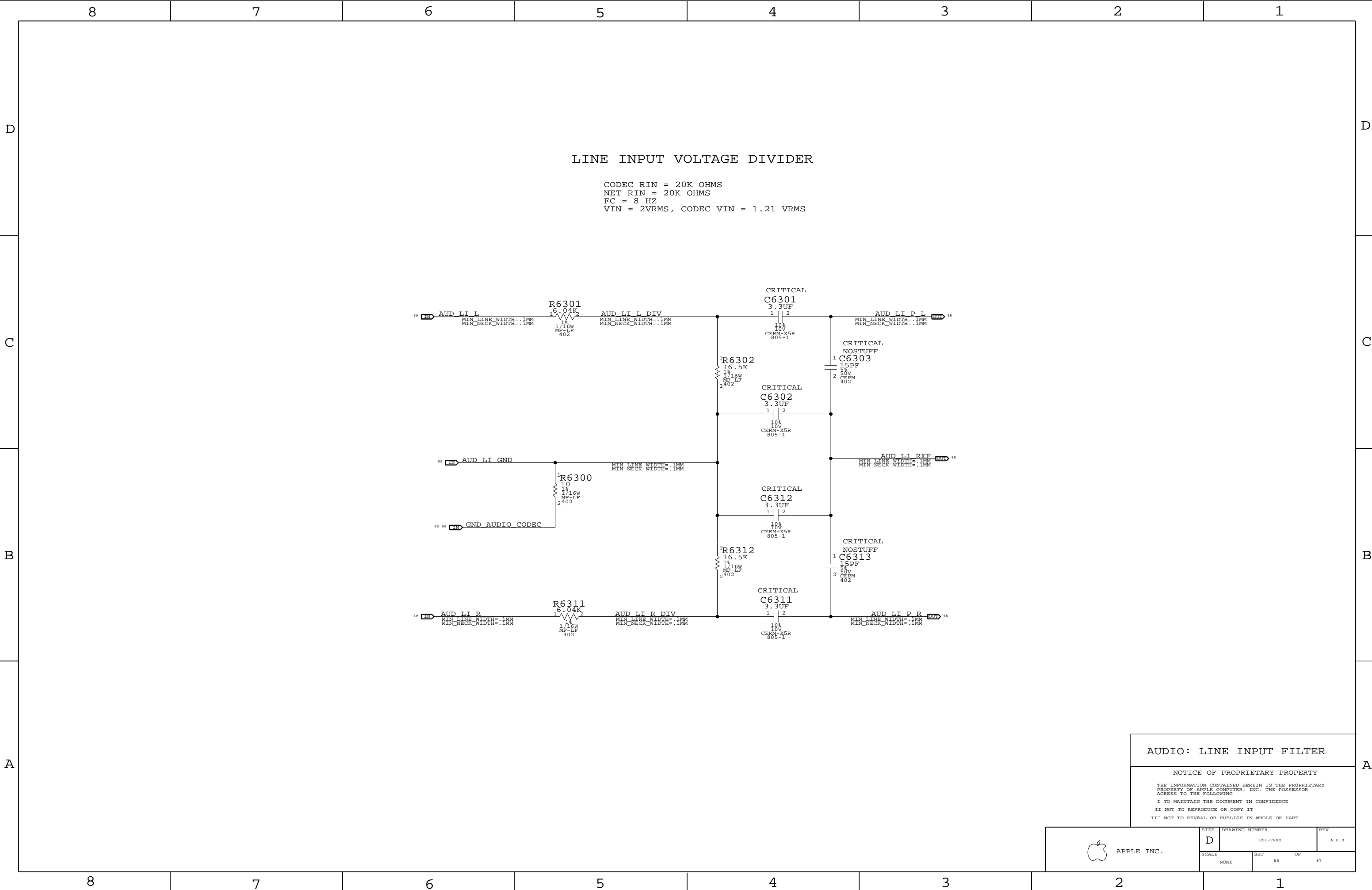
II NOT TO REPRODUCE OR COPY IT

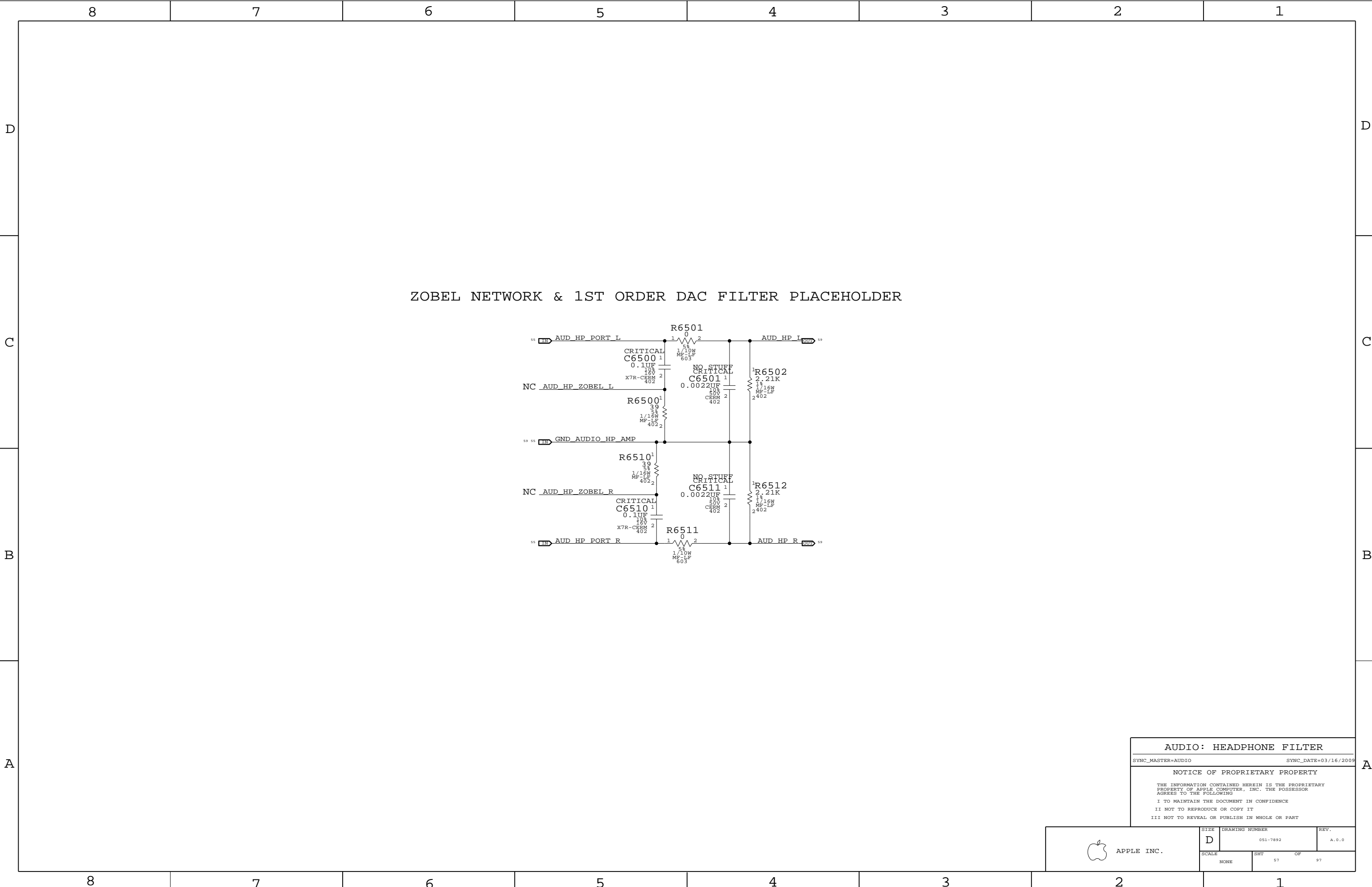
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



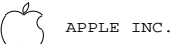
SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	54	97



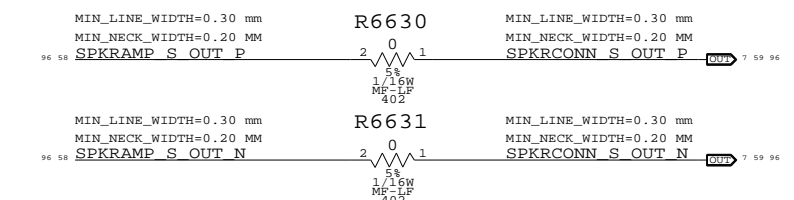
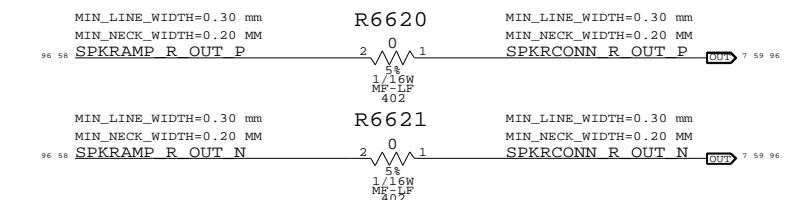
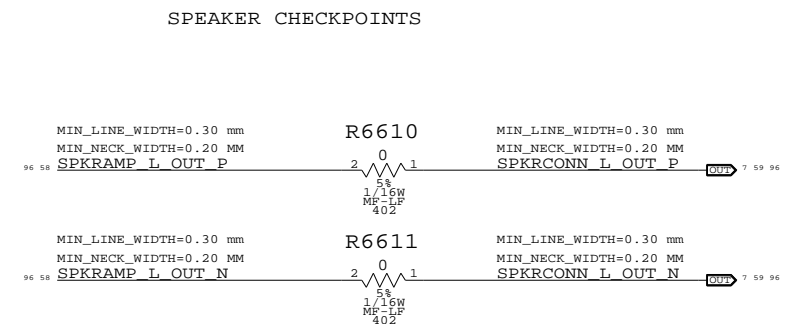
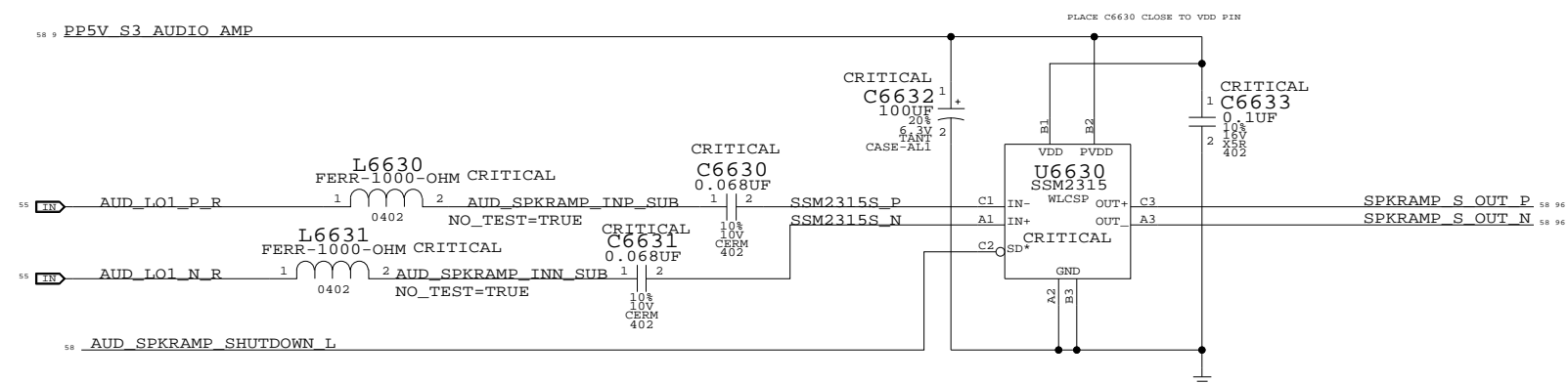
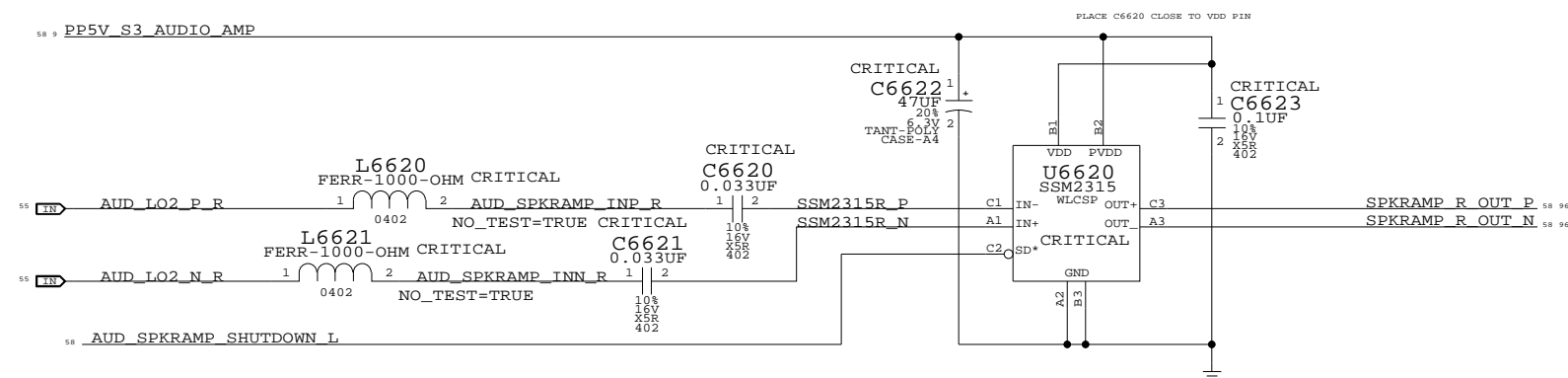
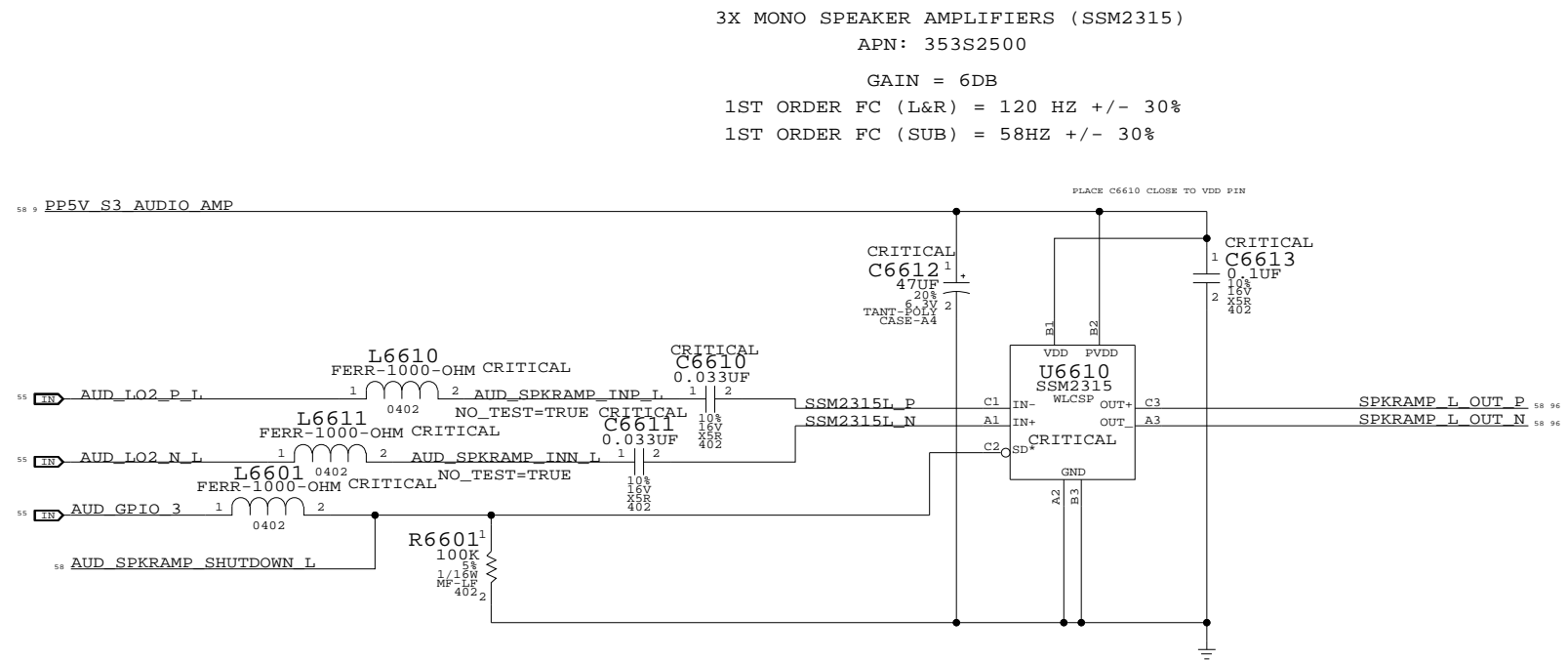




AUDIO: HEADPHONE FILTER		
SYNC_MASTER=AUDIO		SYNC_DATE=03/16/2009
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SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	57	97



APPLE INC.



AUDIO: SPEAKER AMP

SYNC_MASTER=AUDIO SYNC_DATE=03/16/2009

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SIZE
D

DRAWING NUMBER	051-789
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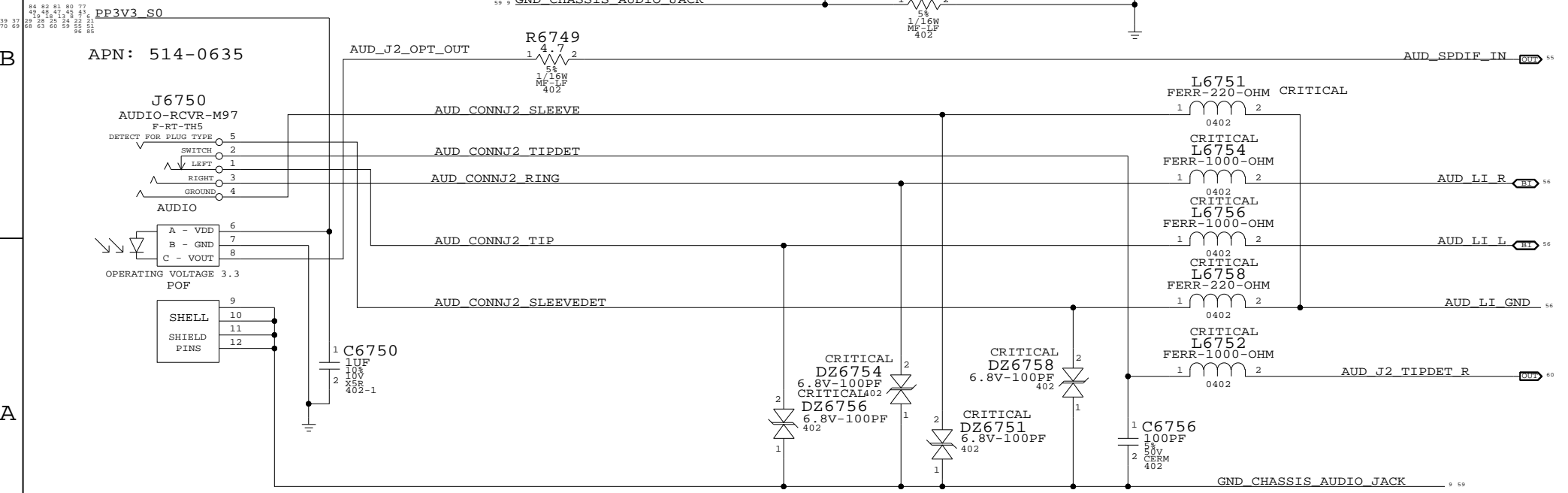
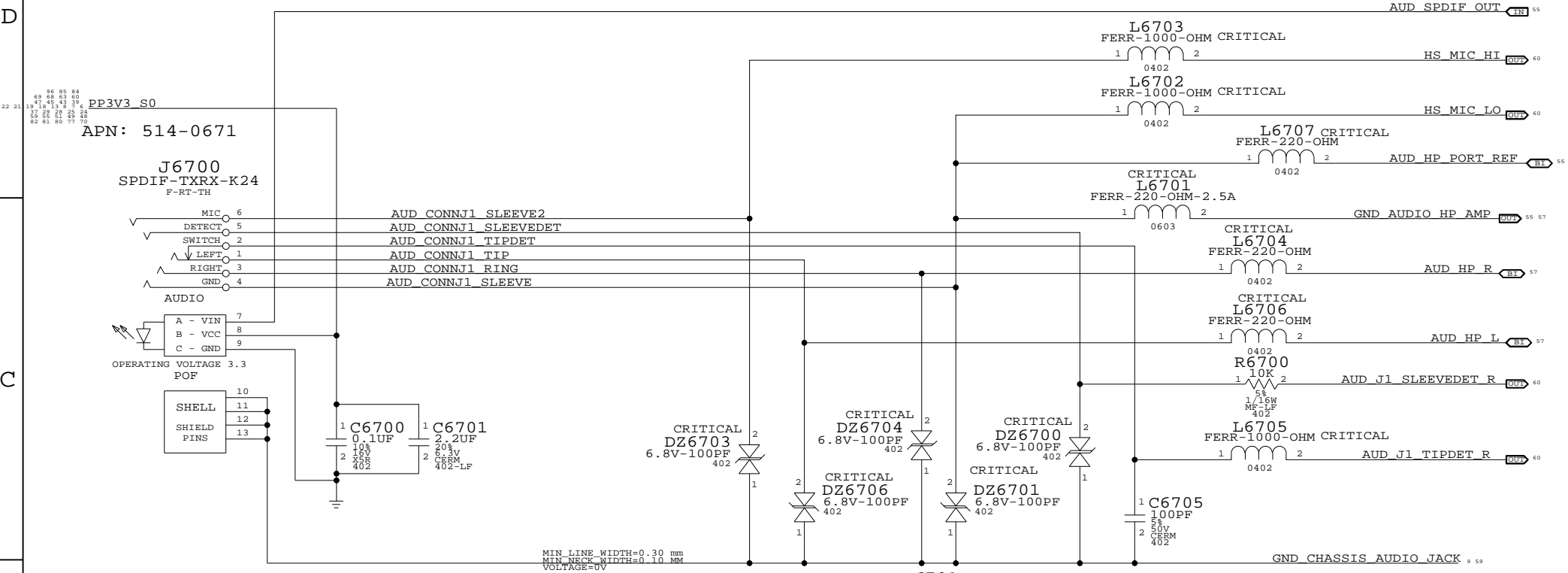
A.O.O

SCALE	NON
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SHT	
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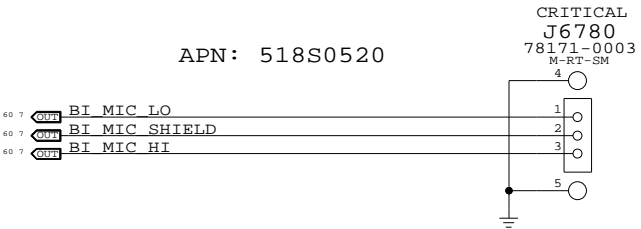
03

AUDIO JACK 1 LO/HP JACK, SPDIF TX



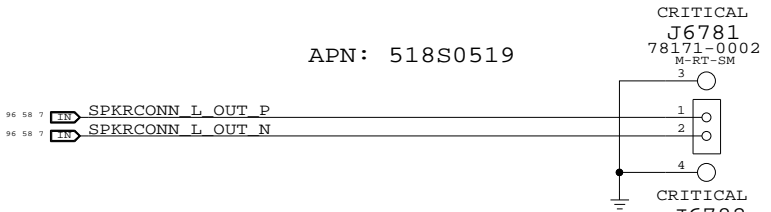
MIC CONNECTOR

APN: 518S0520

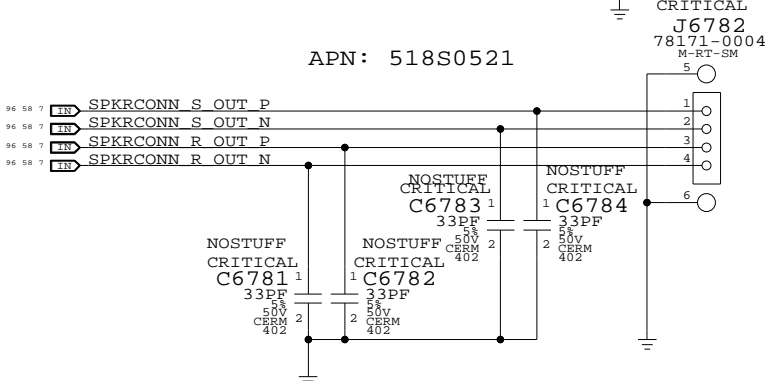


SPEAKER CONNECTOR

APN: 518S0519



APN: 518S0521



AUDIO: JACKS

SYNC_MASTER=AUDIO SYNC_DATE=03/16/2009

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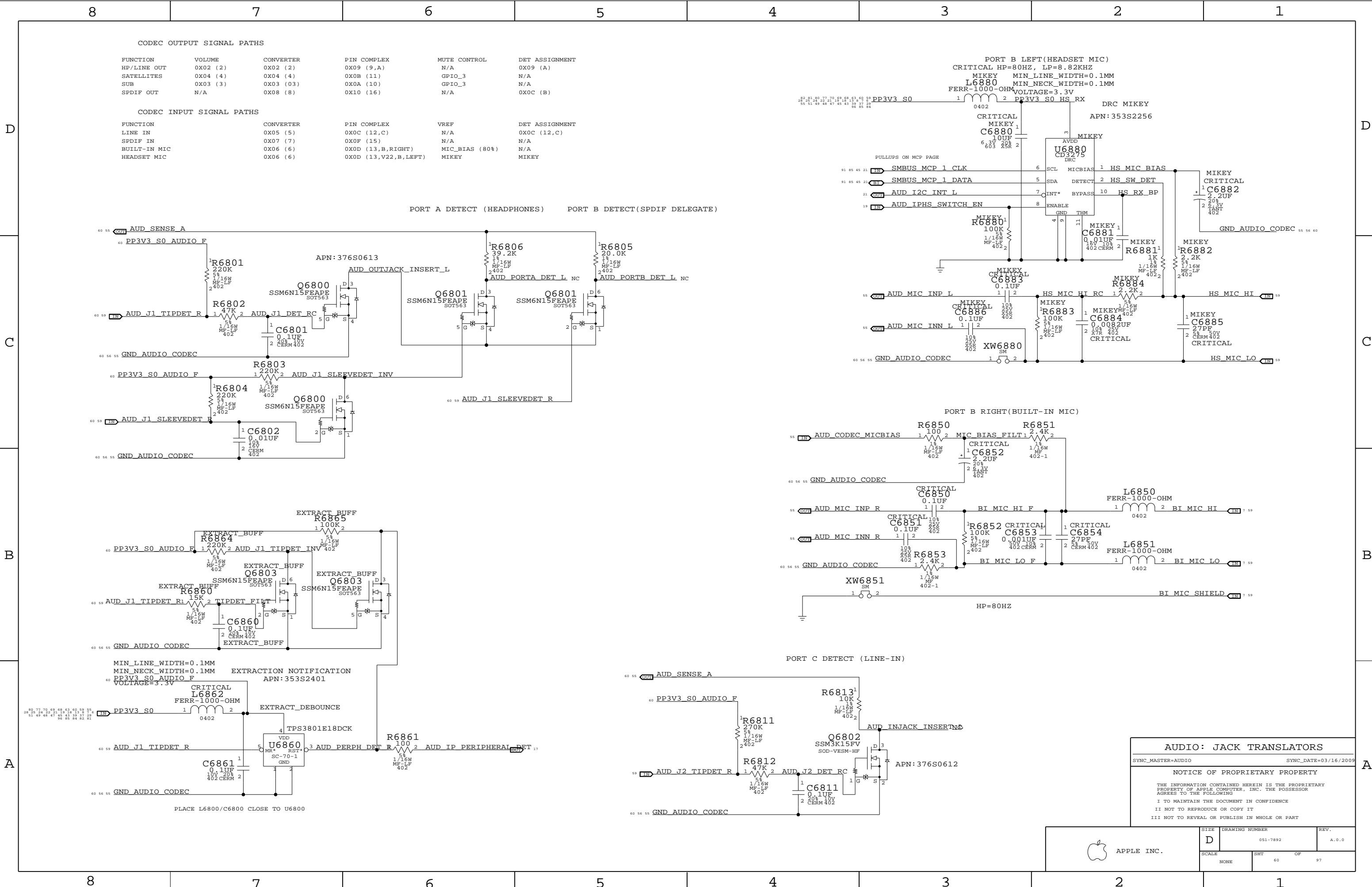
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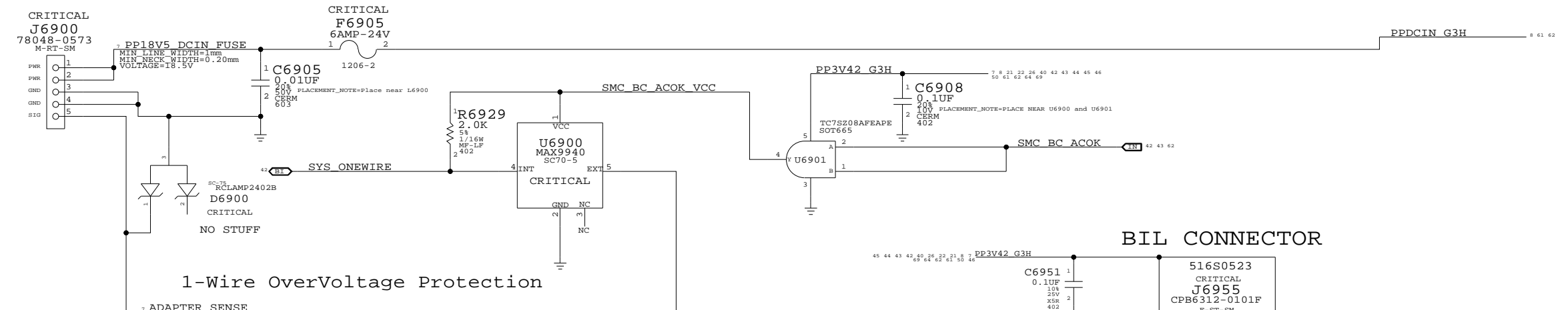
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	59	97

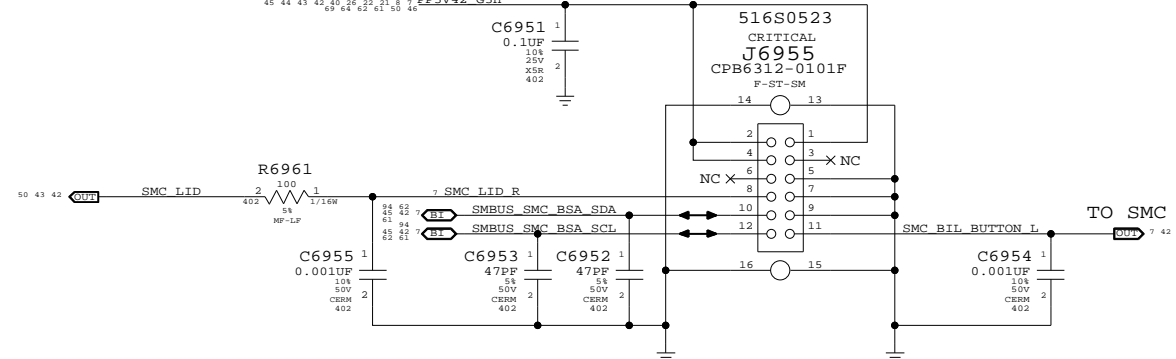


MagSafe DC Power Jack



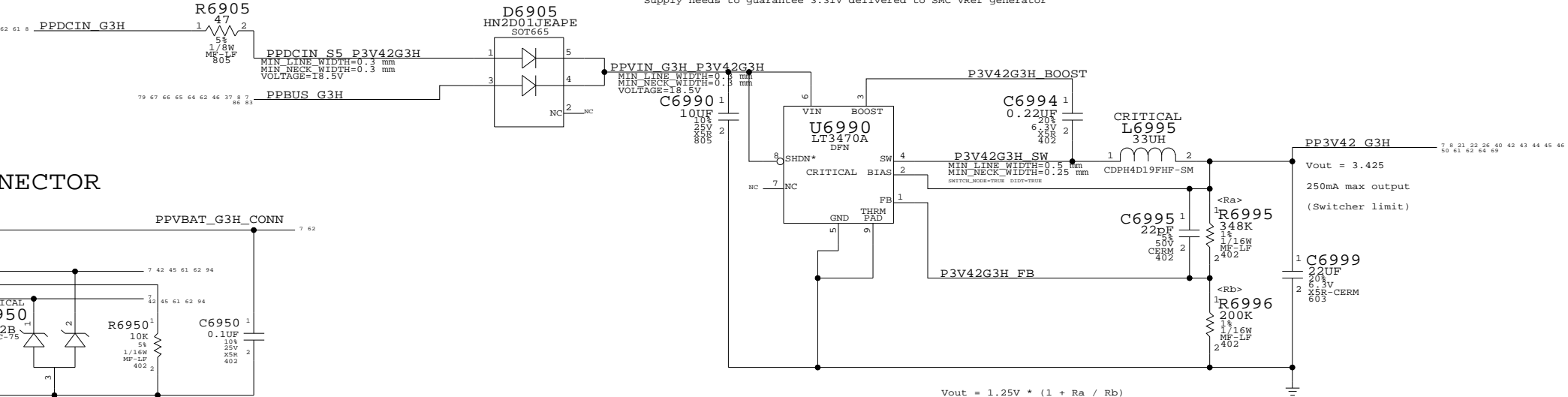
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

BIL CONNECTOR

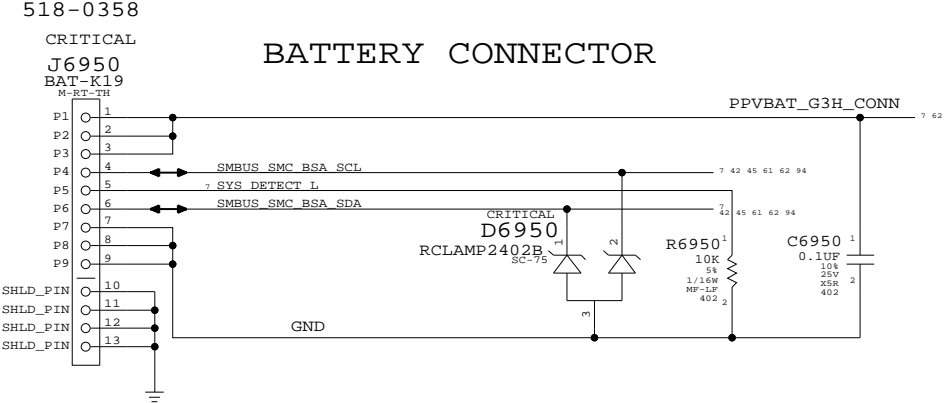


3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

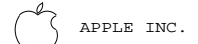


BATTERY CONNECTOR

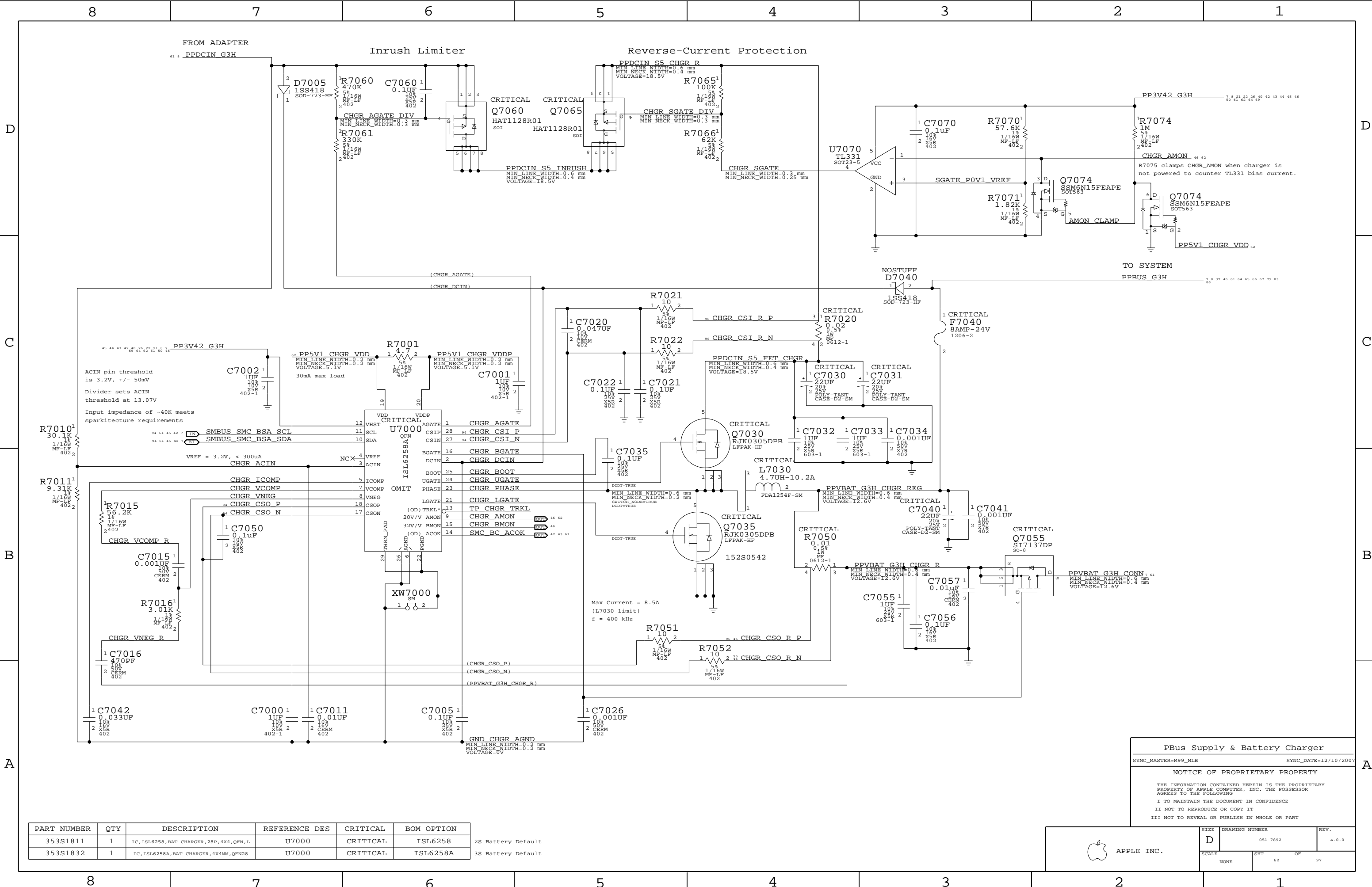


DC-In & Battery Connectors		
SYNC_MASTER=YUN_K19_MLB		SYNC_DATE=12/16/2008
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DRAWING NUMBER		REV.	
051-7892		A.0.0	
SCALE		SHT	
NONE		61 OF 97	



APPLE INC.



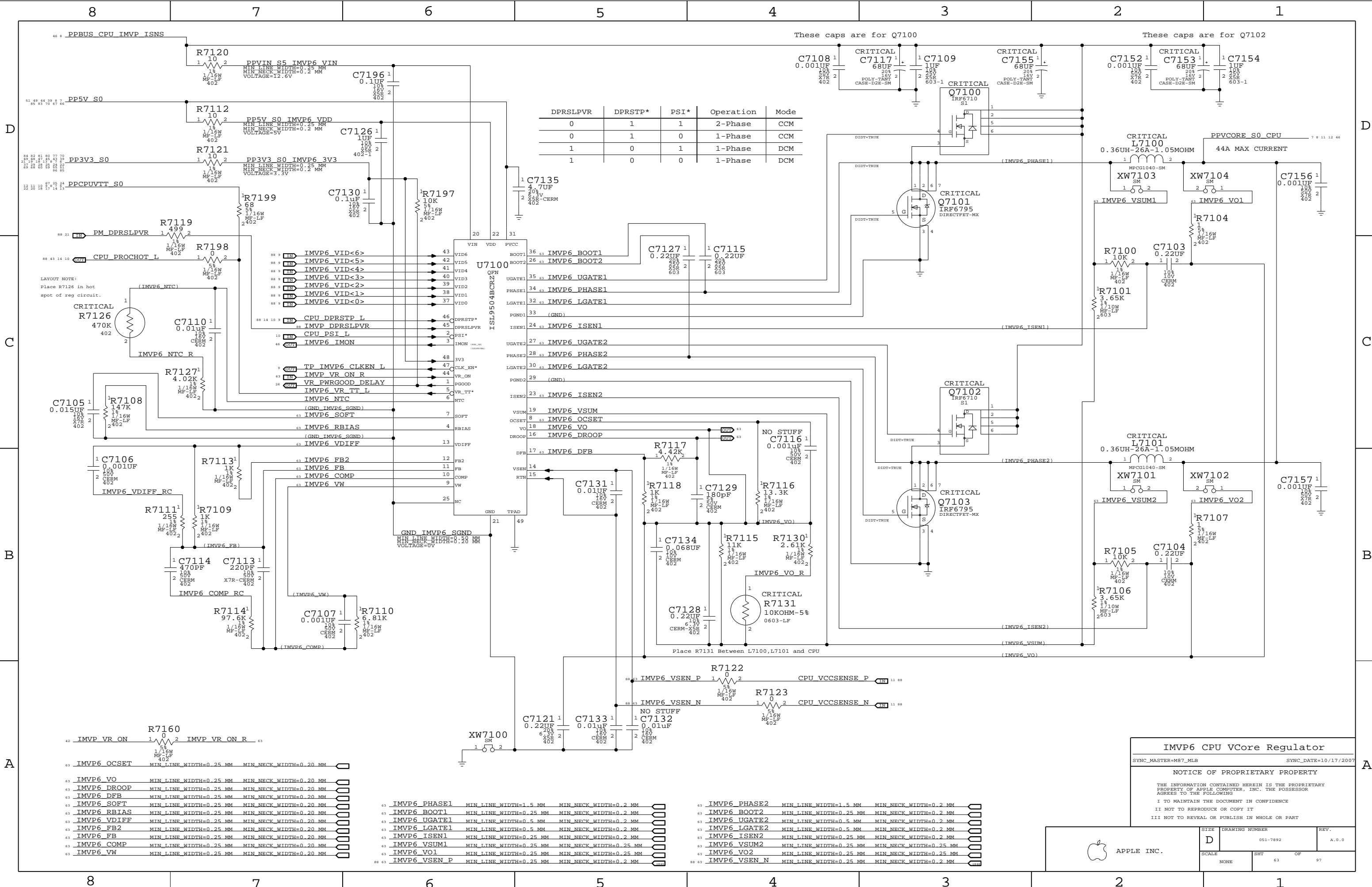
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S1811	1	IC, ISL6258A, BAT CHARGER, 28P, 4X4, QFN, L	U7000	CRITICAL	ISL6258
353S1832	1	IC, ISL6258A, BAT CHARGER, 4X4MM, QFN28	U7000	CRITICAL	ISL6258A

2S Battery Default
3S Battery Default

PBus Supply & Battery Charger
SYNC_MASTER=M99_MLB
SYNC_DATE=12/10/2007
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SCALE: NONE
SHT: 62
OF: 97
DRAWING NUMBER: 051-7892
REV.: A.0.0



DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

IMVP6 PHASE1	MIN LINE WIDTH=1.5 MM	MIN NECK WIDTH=0.2 MM	IMVP6 PHASE2	MIN LINE WIDTH=1.5 MM	MIN NECK WIDTH=0.2 MM
IMVP6 BOOT1	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.2 MM	IMVP6 BOOT2	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.2 MM
IMVP6 UGATE1	MIN LINE WIDTH=0.5 MM	MIN NECK WIDTH=0.2 MM	IMVP6 UGATE2	MIN LINE WIDTH=0.5 MM	MIN NECK WIDTH=0.2 MM
IMVP6 LGATE1	MIN LINE WIDTH=0.5 MM	MIN NECK WIDTH=0.2 MM	IMVP6 LGATE2	MIN LINE WIDTH=0.5 MM	MIN NECK WIDTH=0.2 MM
IMVP6 ISEN1	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.2 MM	IMVP6 ISEN2	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.2 MM
IMVP6 VSUM1	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.25 MM	IMVP6 VSUM2	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.25 MM
IMVP6 VO1	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.25 MM	IMVP6 VO2	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.25 MM
IMVP6 VSEN_P	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.2 MM	IMVP6 VSEN_N	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.2 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

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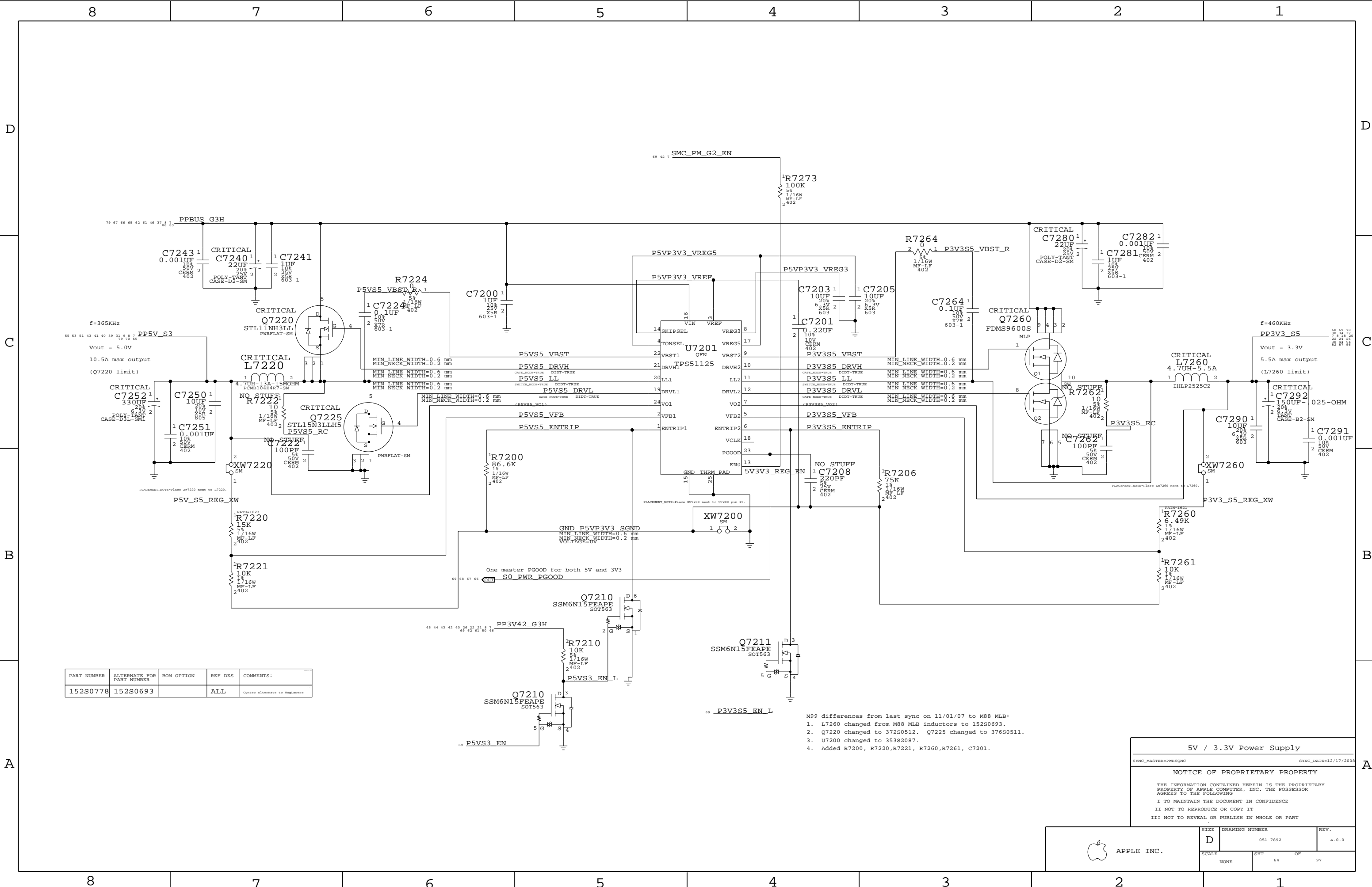
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APPLE INC.

D 051-7892 A.0.0

SCALE SHT 63 OF 97



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	Cyrcse alternate to MapLayers

- M99 differences from last sync on 11/01/07 to M88 MLB:
1. L7260 changed from M88 MLB inductors to 152S0693.
 2. Q7220 changed to 372S0512. Q7225 changed to 376S0511.
 3. U7200 changed to 353S2087.
 4. Added R7200, R7220, R7221, R7260, R7261, C7201.

5V / 3.3V Power Supply

SYNC_MASTER=PWR5QNC

SYNC_DATE=12/17/2008

NOTICE OF PROPRIETARY PROPERTY

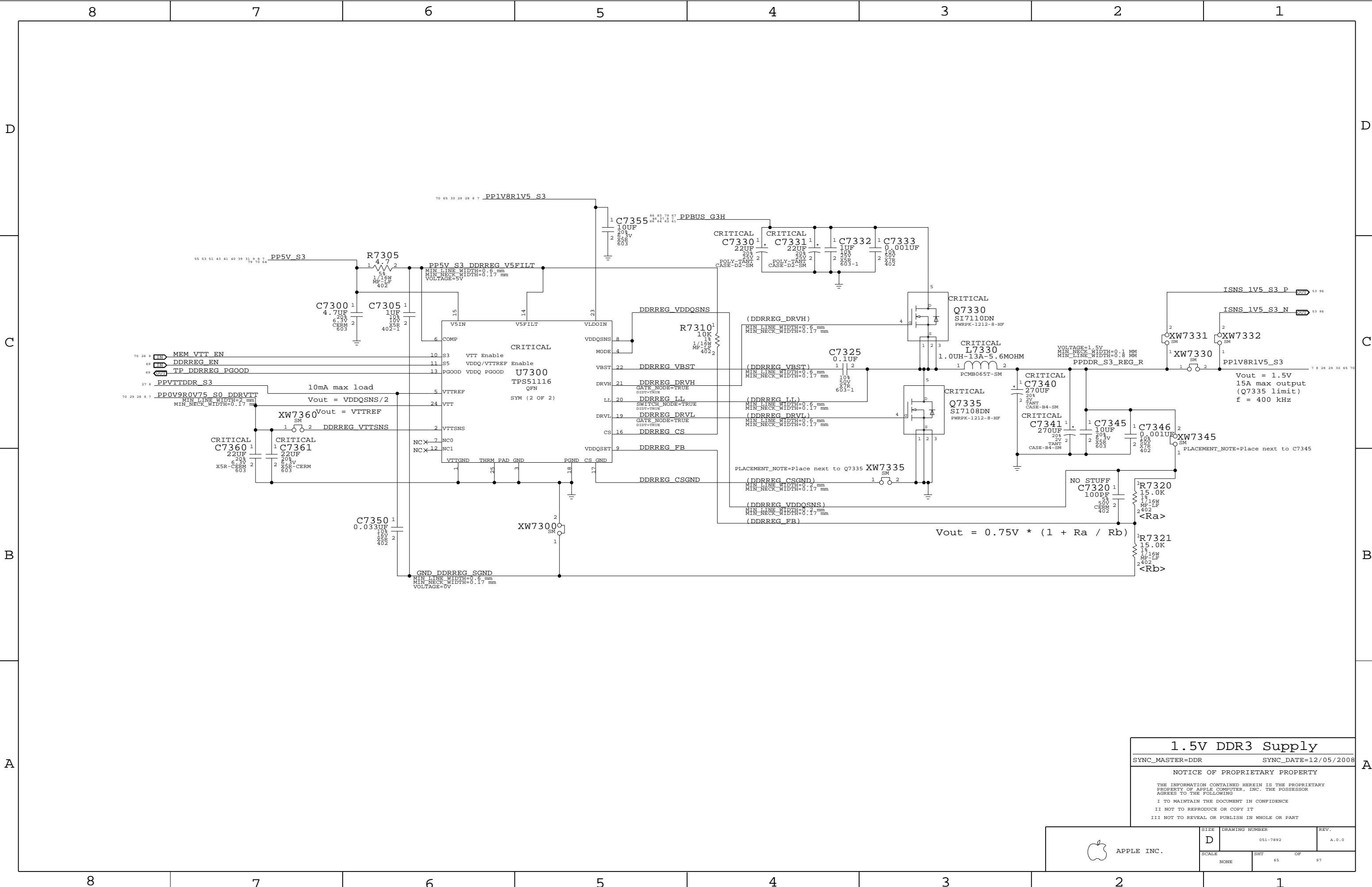
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	D	051-7892	A.0.0
SCALE		SHT	OF
NONE		64	97



1.5V DDR3 Supply

SYNC_MASTER=DDR

SYNC_DATE=12/05/2008

NOTICE OF PROPRIETARY PROPERTY

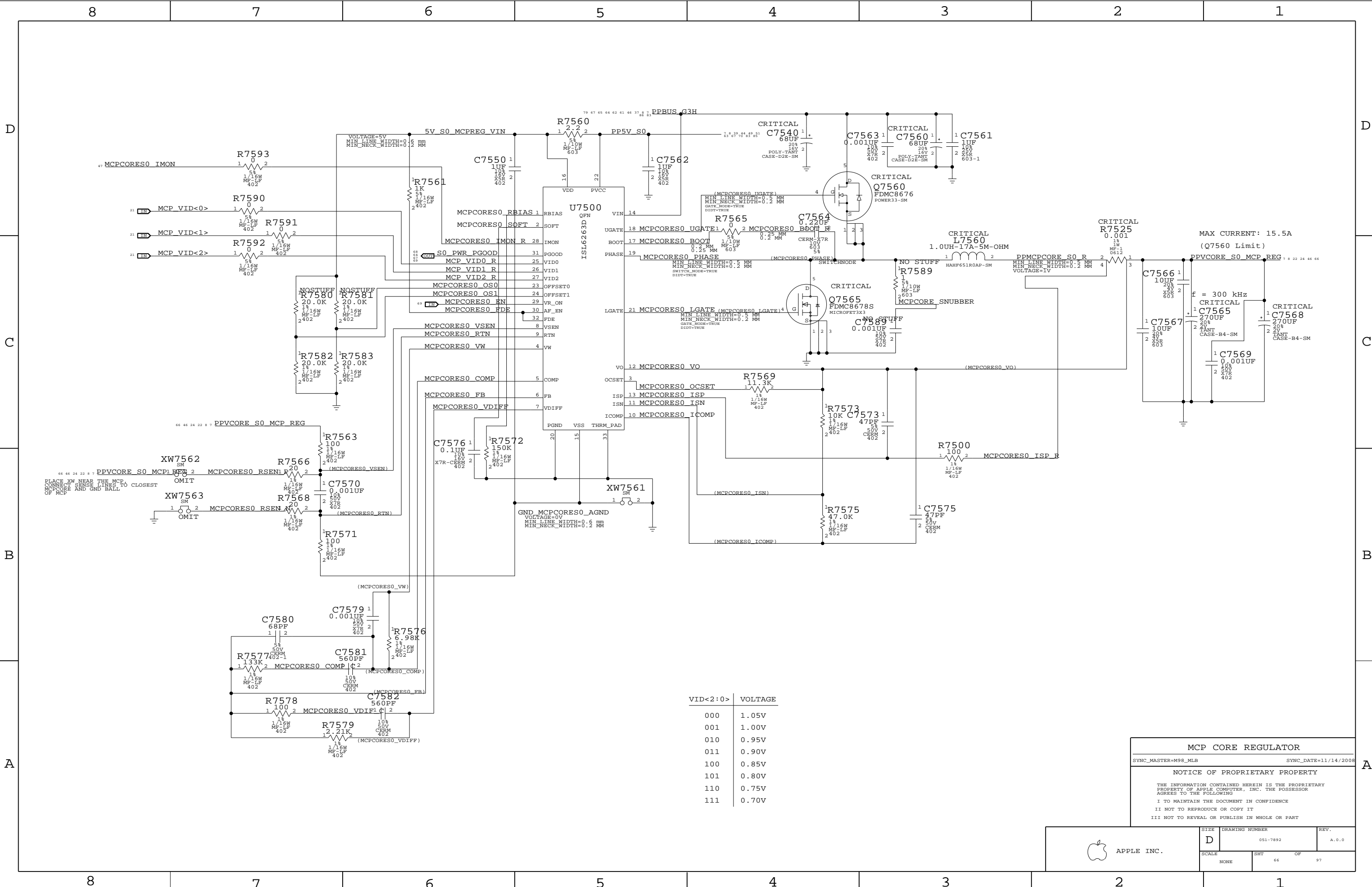
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	D	051-7892	A.0.0
SCALE		SHT	OF
NONE		65	97



VID<2:0>	VOLTAGE
000	1.05V
001	1.00V
010	0.95V
011	0.90V
100	0.85V
101	0.80V
110	0.75V
111	0.70V

MCP CORE REGULATOR

SYNC_MASTER=M98_MLB SYNC_DATE=11/14/2008

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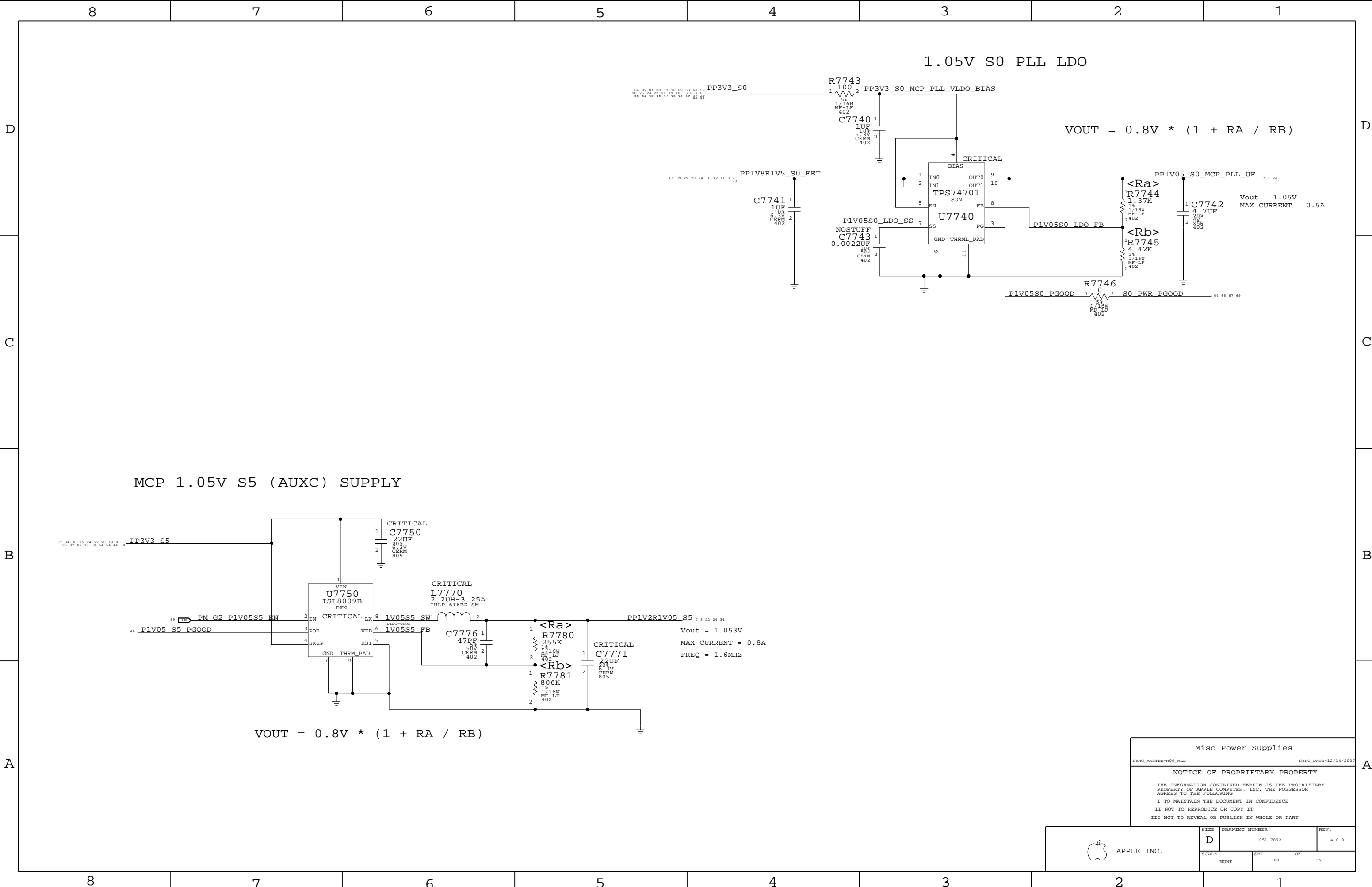
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	66	97



Misc Power Supplies

SYNC_MASTER=M99_MLS SYNC_DATE=12/14/2007

NOTICE OF PROPRIETARY PROPERTY

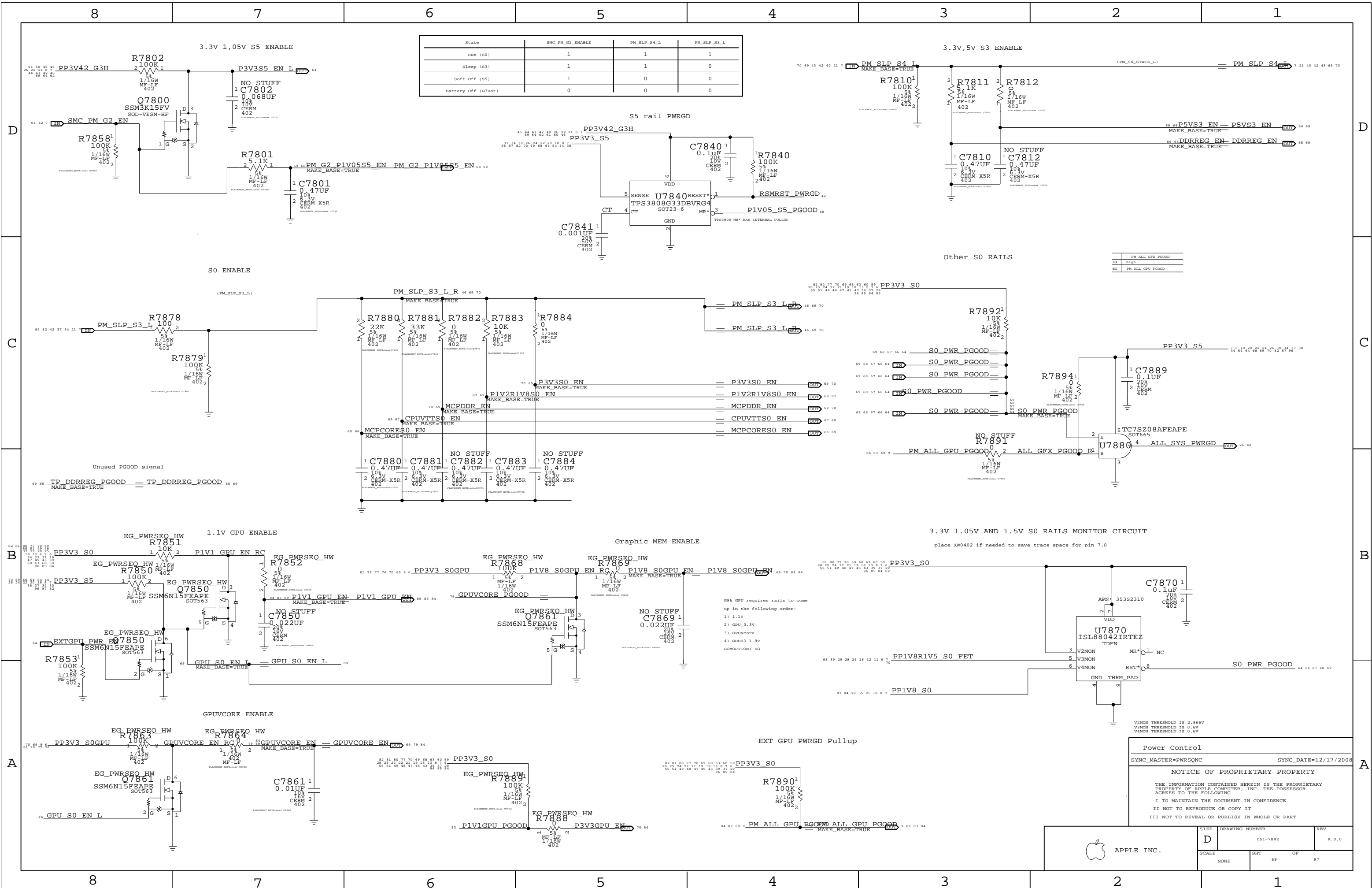
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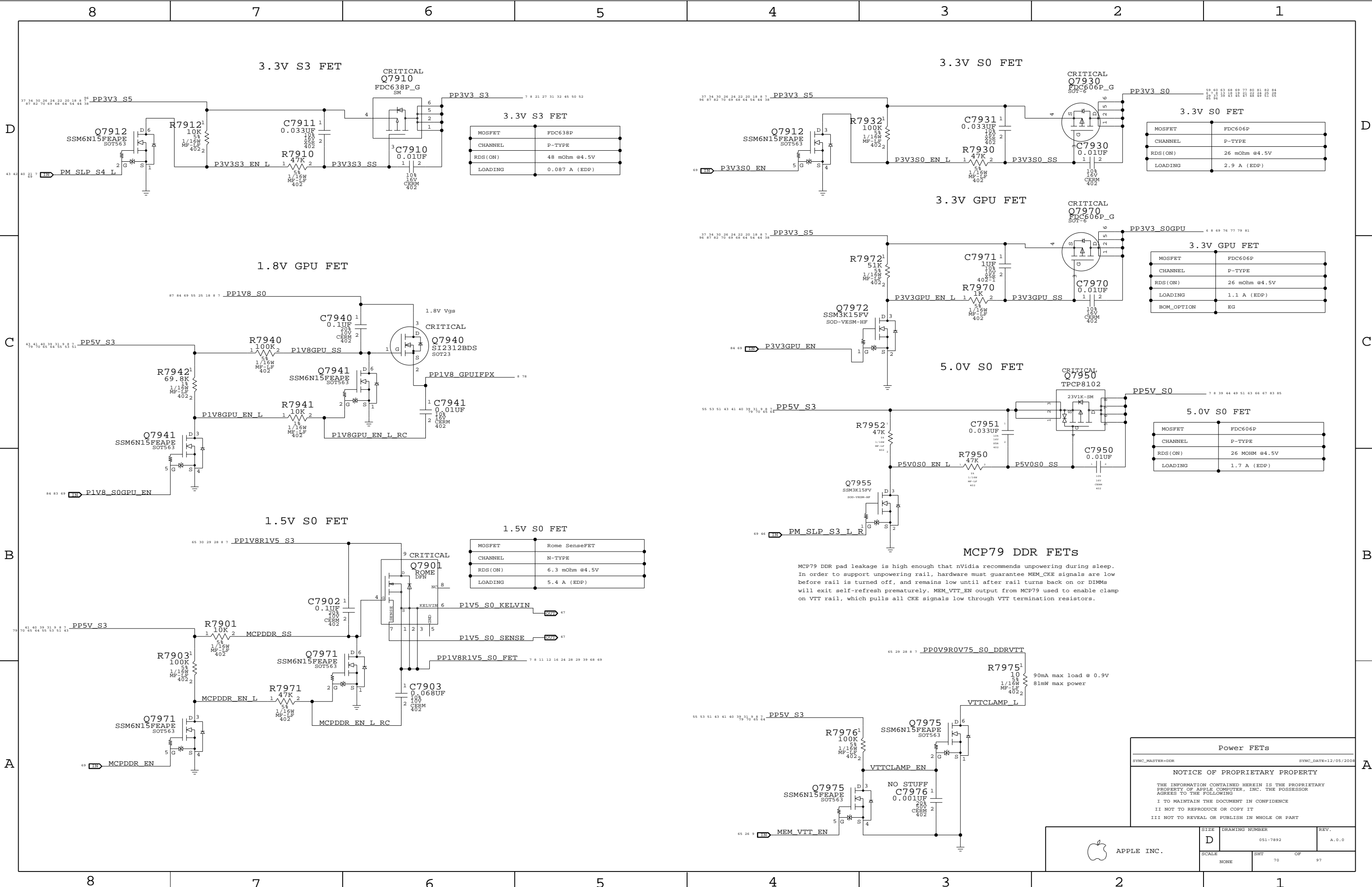
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7892	A.0.0
SCALE		SHT	OF
NONE		68	97





MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.087 A (EDP)

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	2.9 A (EDP)

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	1.1 A (EDP)
BOM_OPTION	EG

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.7 A (EDP)

MOSFET	Rome SenseFET
CHANNEL	N-TYPE
RDS(ON)	6.3 mOhm @4.5V
LOADING	5.4 A (EDP)

MCP79 DDR pad leakage is high enough that nvidia recommends unpowering during sleep. In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low before rail is turned off, and remains low until after rail turns back on or DIMMs will exit self-refresh prematurely. MEM_VTT_EN output from MCP79 used to enable clamp on VTT rail, which pulls all CKE signals low through VTT termination resistors.

Power FETs		
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7892	A.0.0
SCALE		SHT	OF
NONE		70	97

```
Power aliases required by this page:
- =PP1V2_GPU_PEX_PILLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD
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```
Signal aliases required by this page:
(NONE)
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BOM options provided by this page:
(NONE)
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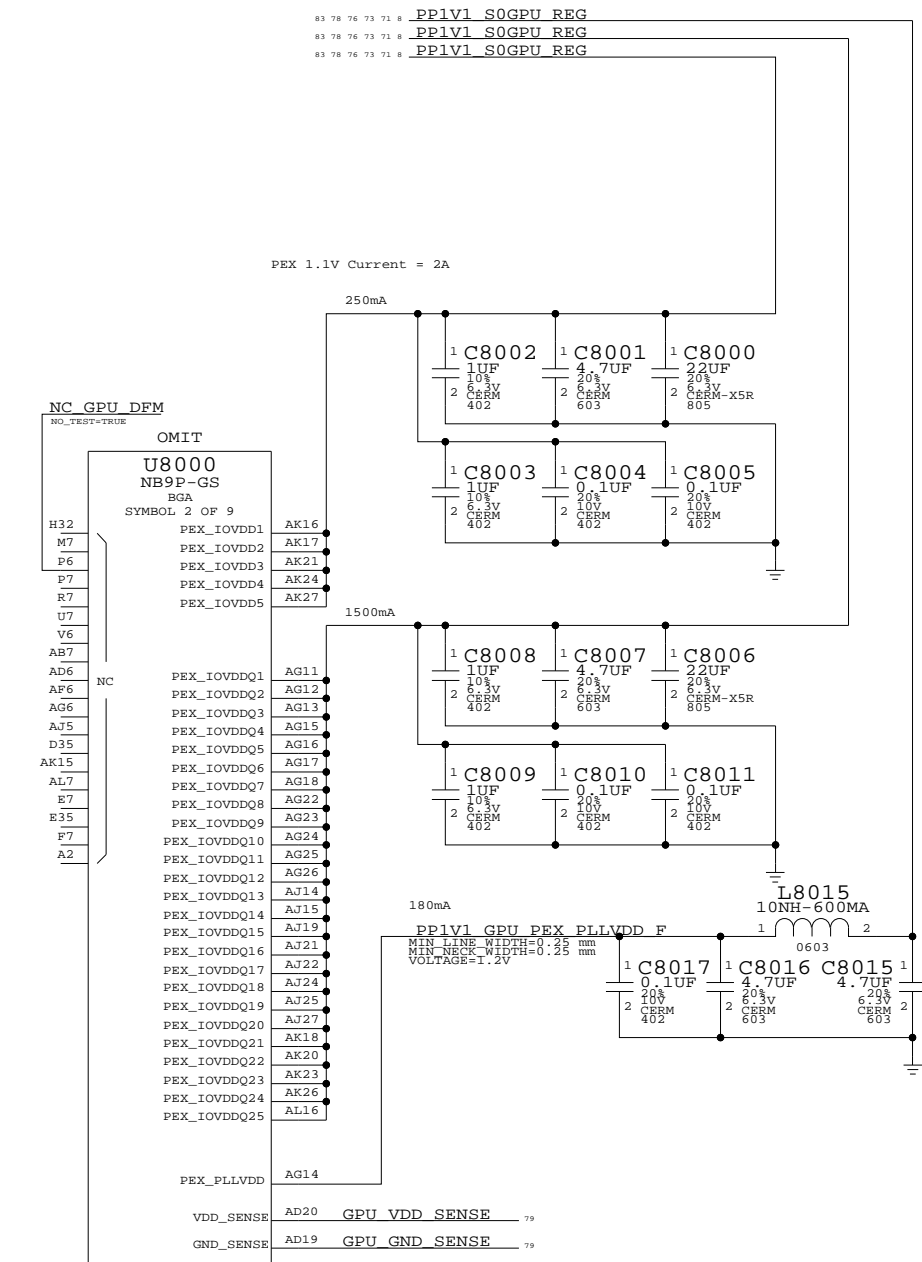
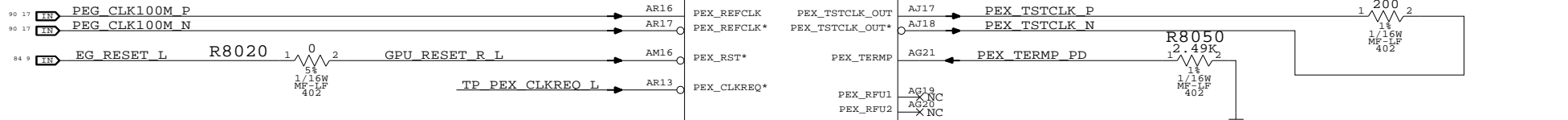


Figure 10: Timing diagram for the PEG D2R C P<0> to PEG D2R C P<15> and PEG D2R C N<0> to PEG D2R C N<15> signals. The diagram shows the relationship between the PEG D2R C P<0> to PEG D2R C P<15> signals and the PEG D2R C N<0> to PEG D2R C N<15> signals. The signals are shown as digital waveforms over time. The PEG D2R C P<0> to PEG D2R C P<15> signals are shown as a sequence of pulses, and the PEG D2R C N<0> to PEG D2R C N<15> signals are shown as a sequence of pulses. The timing diagram is divided into two main sections: the top section shows the PEG D2R C P<0> to PEG D2R C P<15> signals, and the bottom section shows the PEG D2R C N<0> to PEG D2R C N<15> signals. The signals are shown as digital waveforms over time, with the PEG D2R C P<0> to PEG D2R C P<15> signals showing a sequence of pulses and the PEG D2R C N<0> to PEG D2R C N<15> signals showing a sequence of pulses. The timing diagram is divided into two main sections: the top section shows the PEG D2R C P<0> to PEG D2R C P<15> signals, and the bottom section shows the PEG D2R C N<0> to PEG D2R C N<15> signals. The signals are shown as digital waveforms over time, with the PEG D2R C P<0> to PEG D2R C P<15> signals showing a sequence of pulses and the PEG D2R C N<0> to PEG D2R C N<15> signals showing a sequence of pulses.



SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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SIZE	DRAWING NUMBER
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DATE	DRAWING NUMBER
D	000 0000

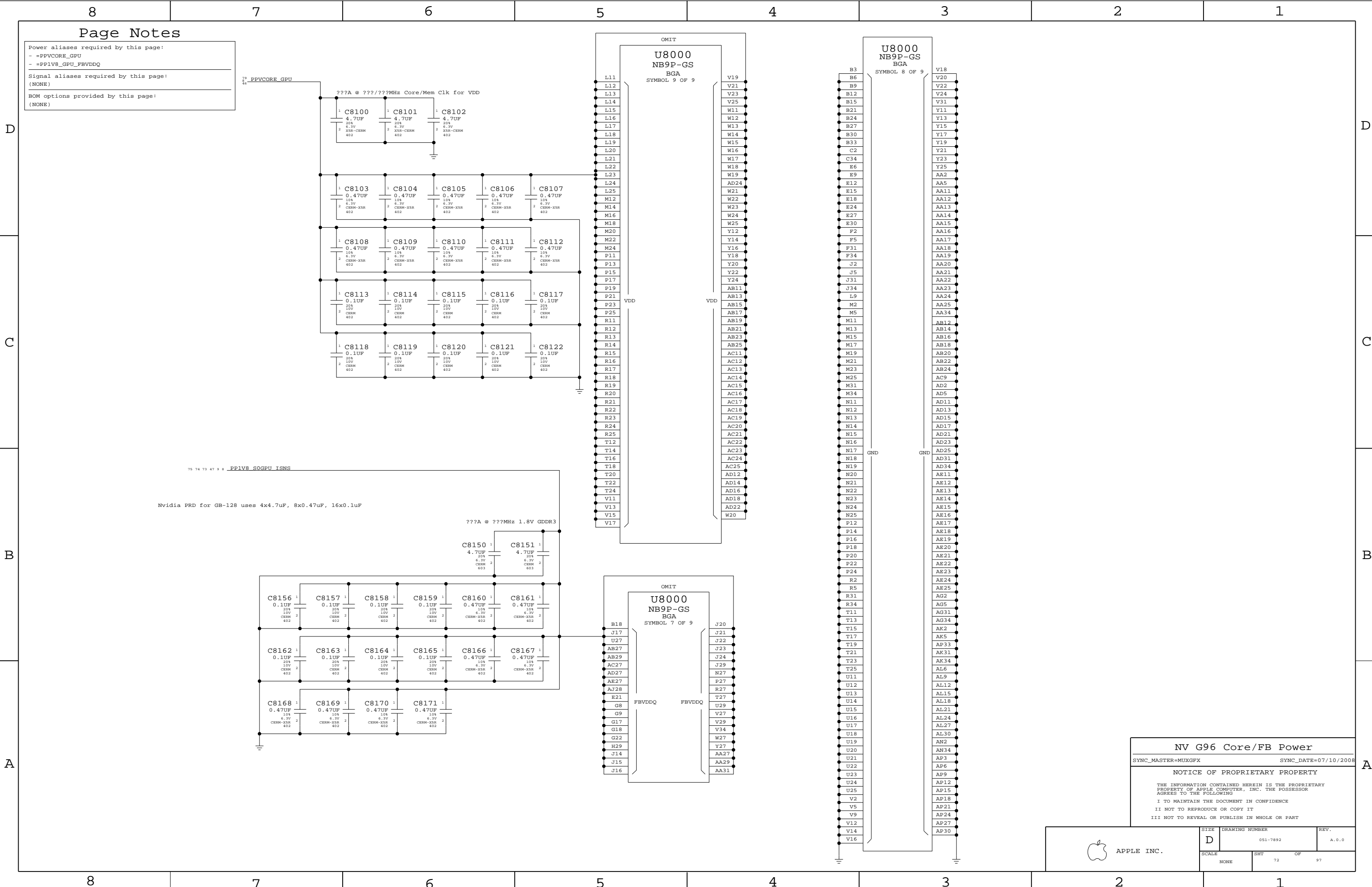
D	051-7892	
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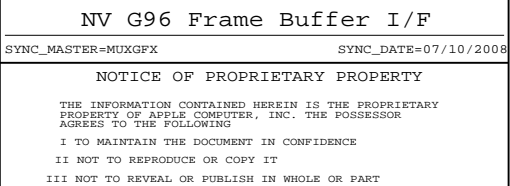
SCALE	SHT	OF
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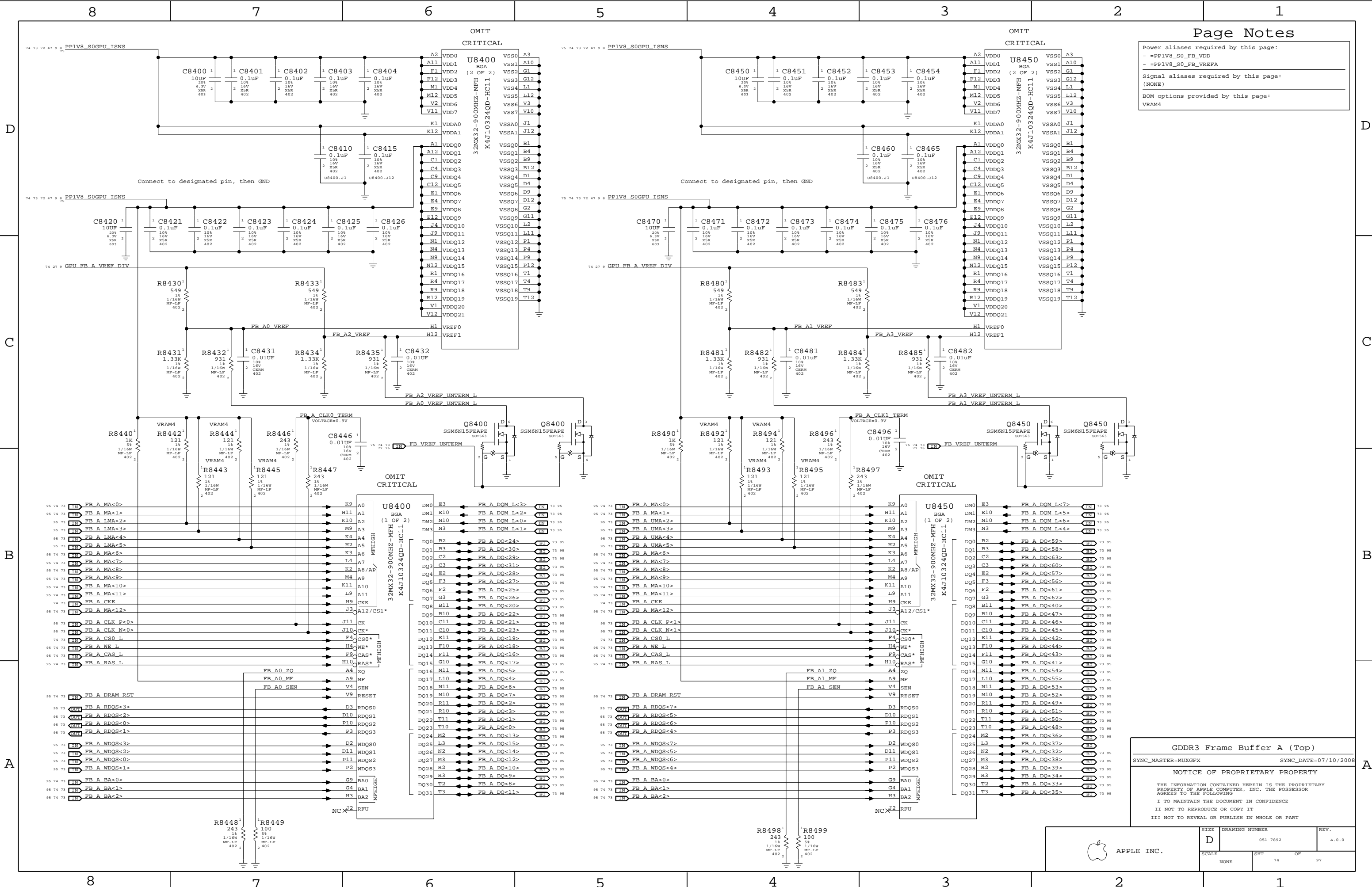
NONE	71	97
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1

[illegible]







Page Notes

Power aliases required by this page:

- =P1V8_S0_FB_VDD
- =P1V8_S0_FB_VREFA

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

VRAM4

GDDR3 Frame Buffer A (Top)

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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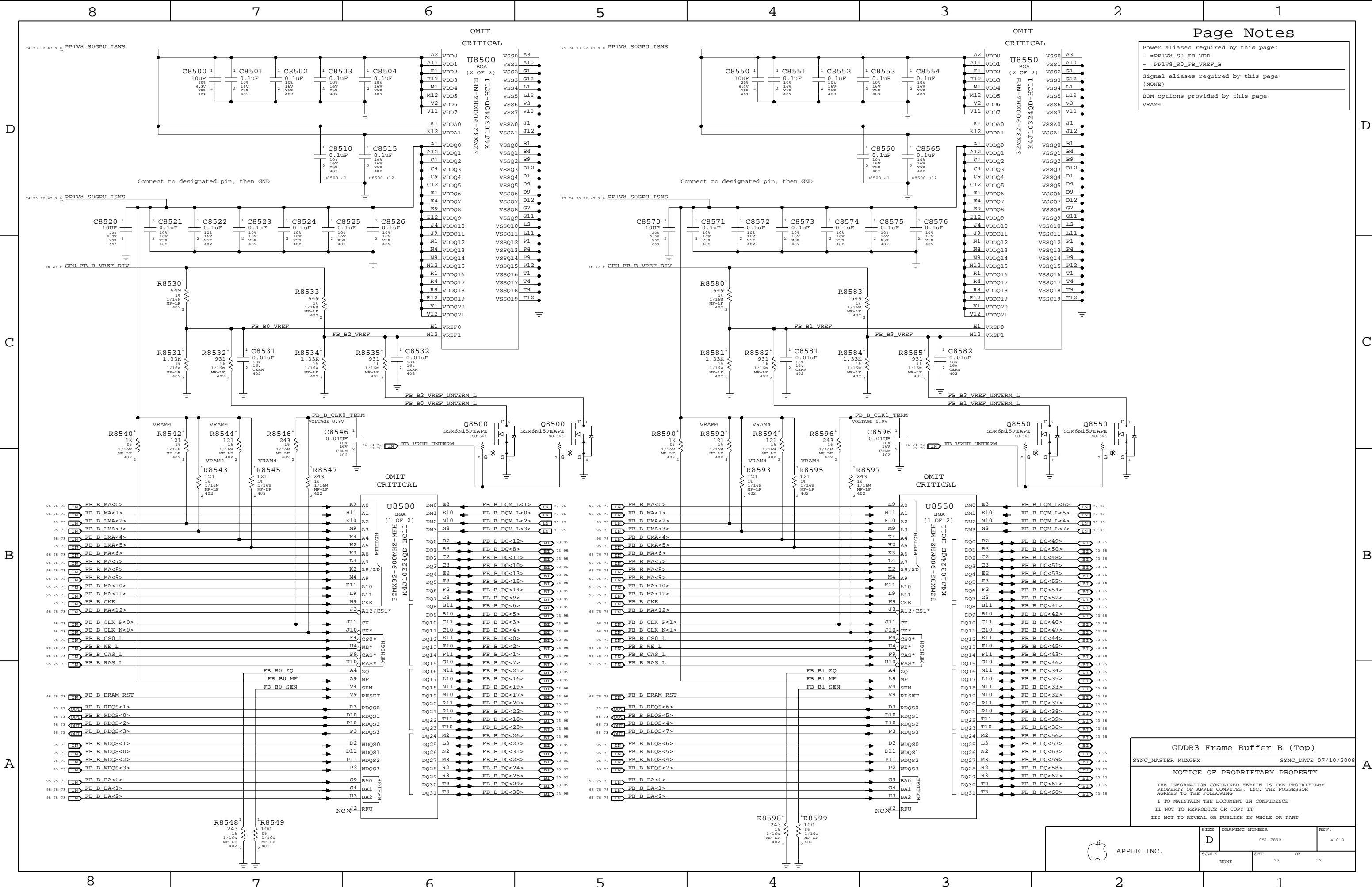
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SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	74	97



Page Notes

Power aliases required by this page:
- =P1V8_S0_FB_VDD
- =P1V8_S0_FB_VREF_B

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4

GDDR3 Frame Buffer B (Top)

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	75	97

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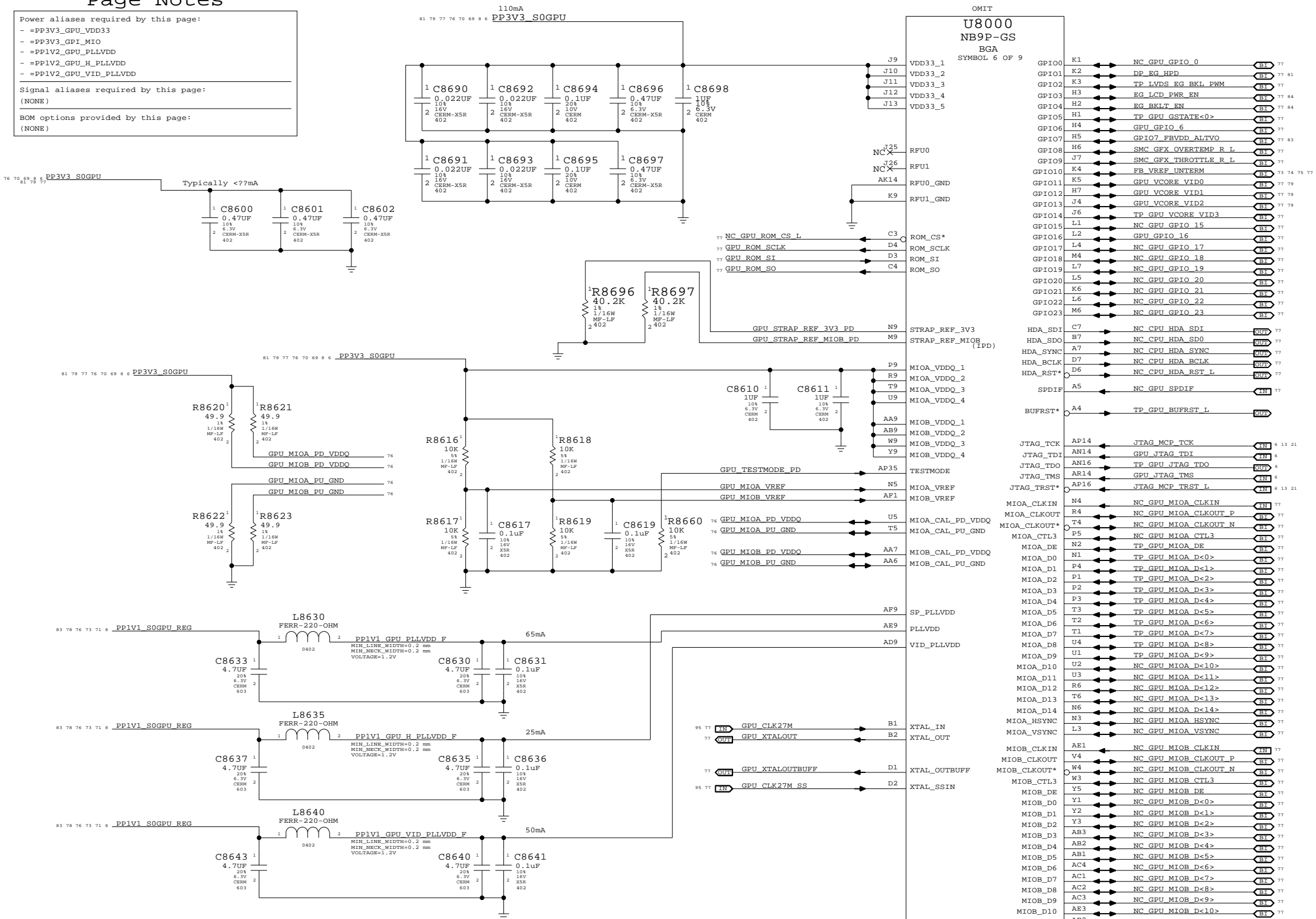
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- =PP3V3_GPU_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



NV G96 GPIO/MIO/Misc

SYNC_MASTER=MUXGFX

SYNC_DATE=07/10/2008

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SIZE

D

DRAWING NUMBER

051-7892

REV.

A.0.0

SCALE

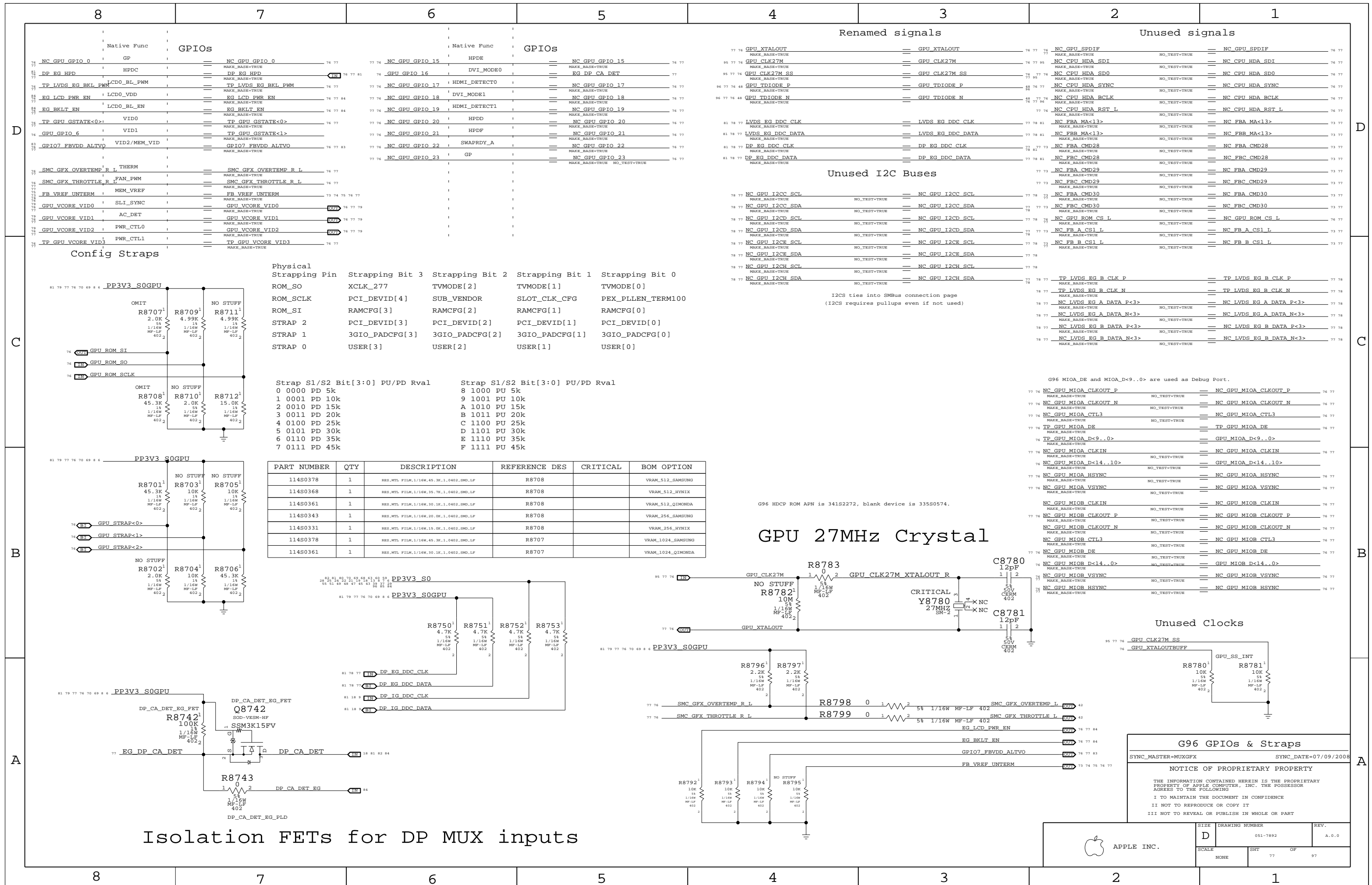
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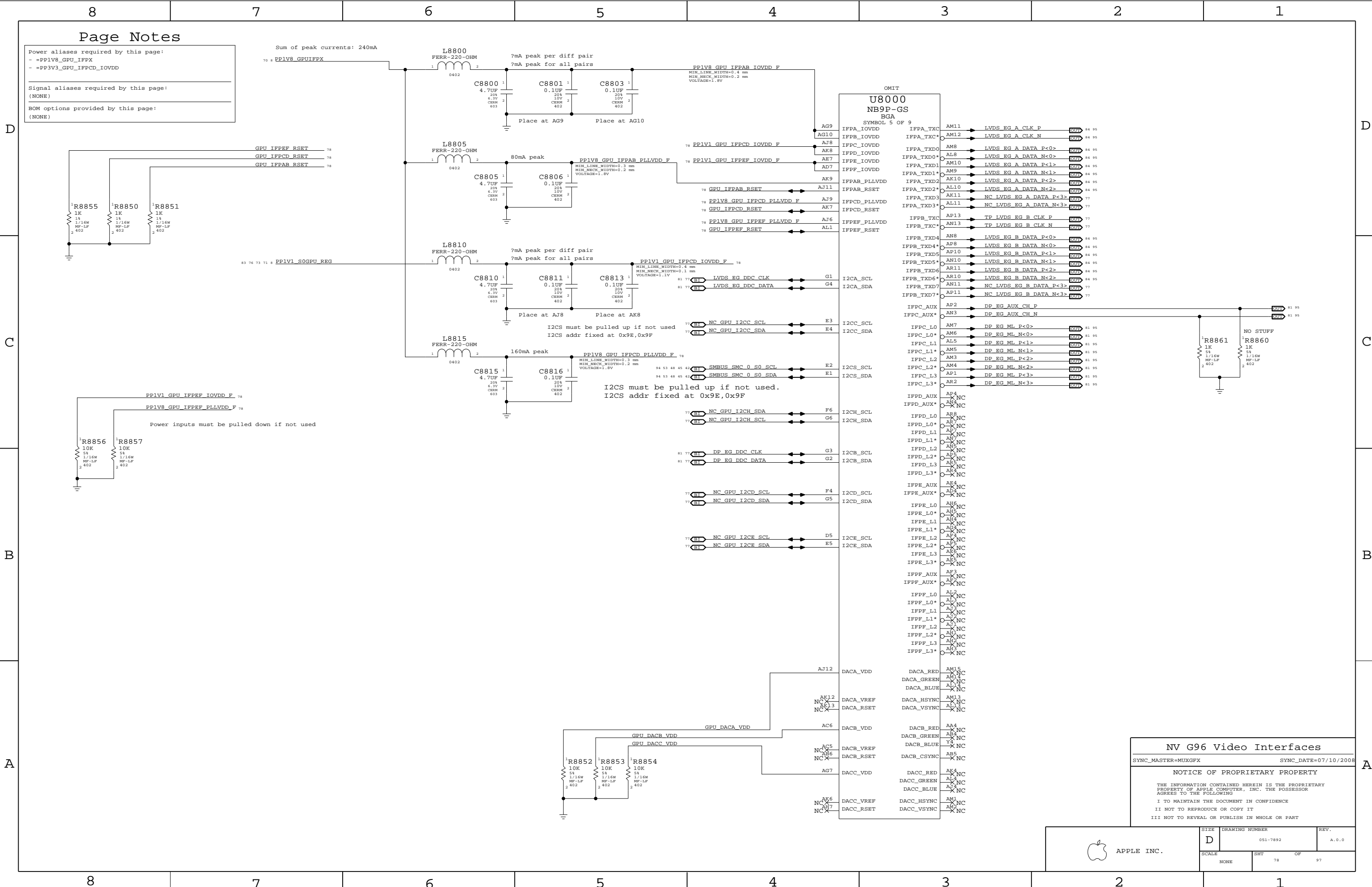
SHT

76

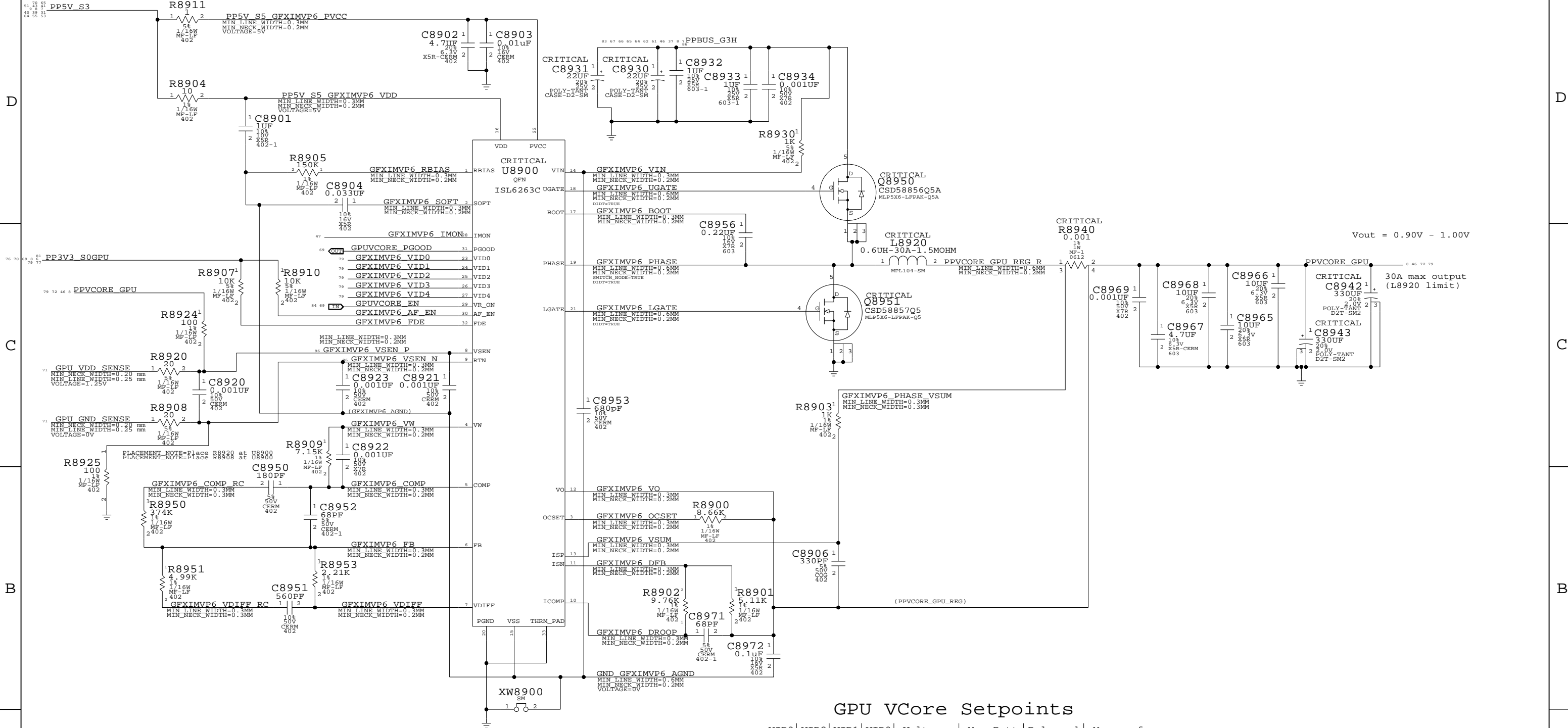
OF

97





GPU VCore Regulator



GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	1	1	1	0.90125V	K19		-
1	1	1	0	0.92700V	-	K19	-
1	0	1	1	1.00425V	-	-	K19

Other VID states may not be valid

K19 Default Vcore Setpoints

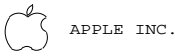
BOM GROUP	BOM OPTIONS
GPUVID_0P90V	GPUVID2_1,GPUVID1_1,GPUVID0_1
GPUVID_1P00V	GPUVID2_0,GPUVID1_1,GPUVID0_1

GPU (G96) CORE SUPPLY

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	79	97

D

C

B

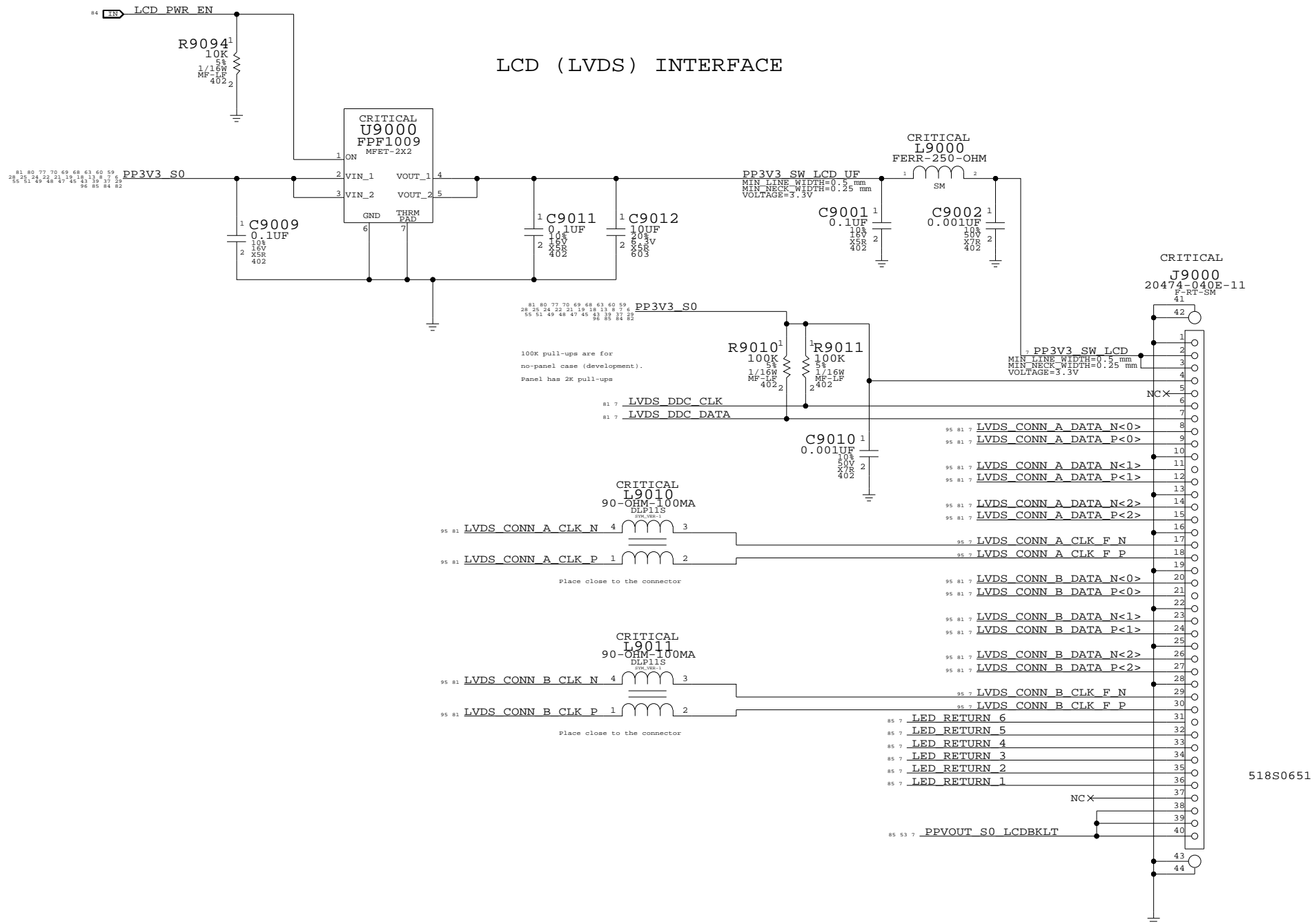
A

D

C

B

A



LVDS Display Connector

SYNC_MASTER=D0R

SYNC_DATE=12/19/2008

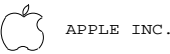
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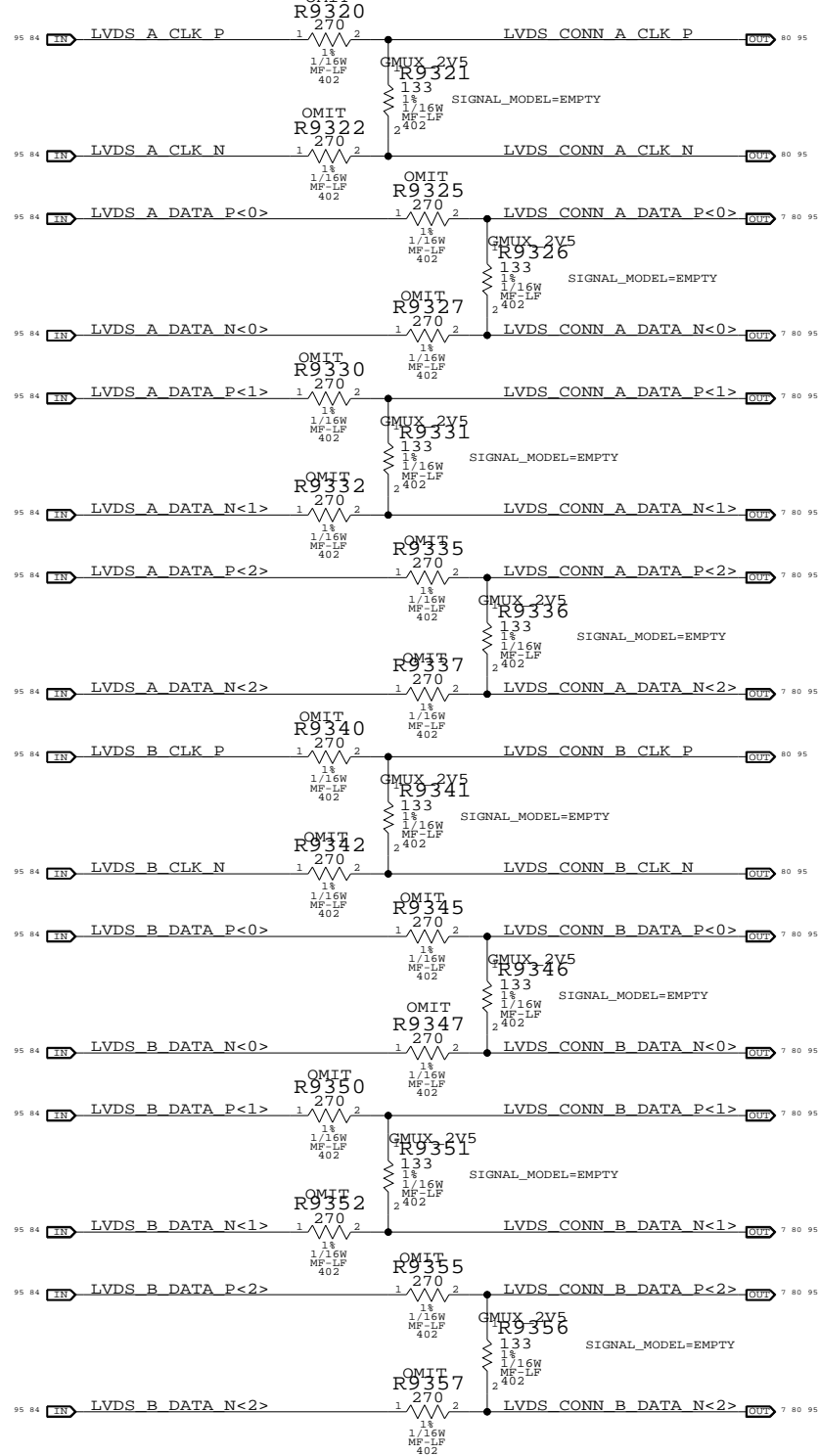
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	80	97

LVDS Transmitter Termination

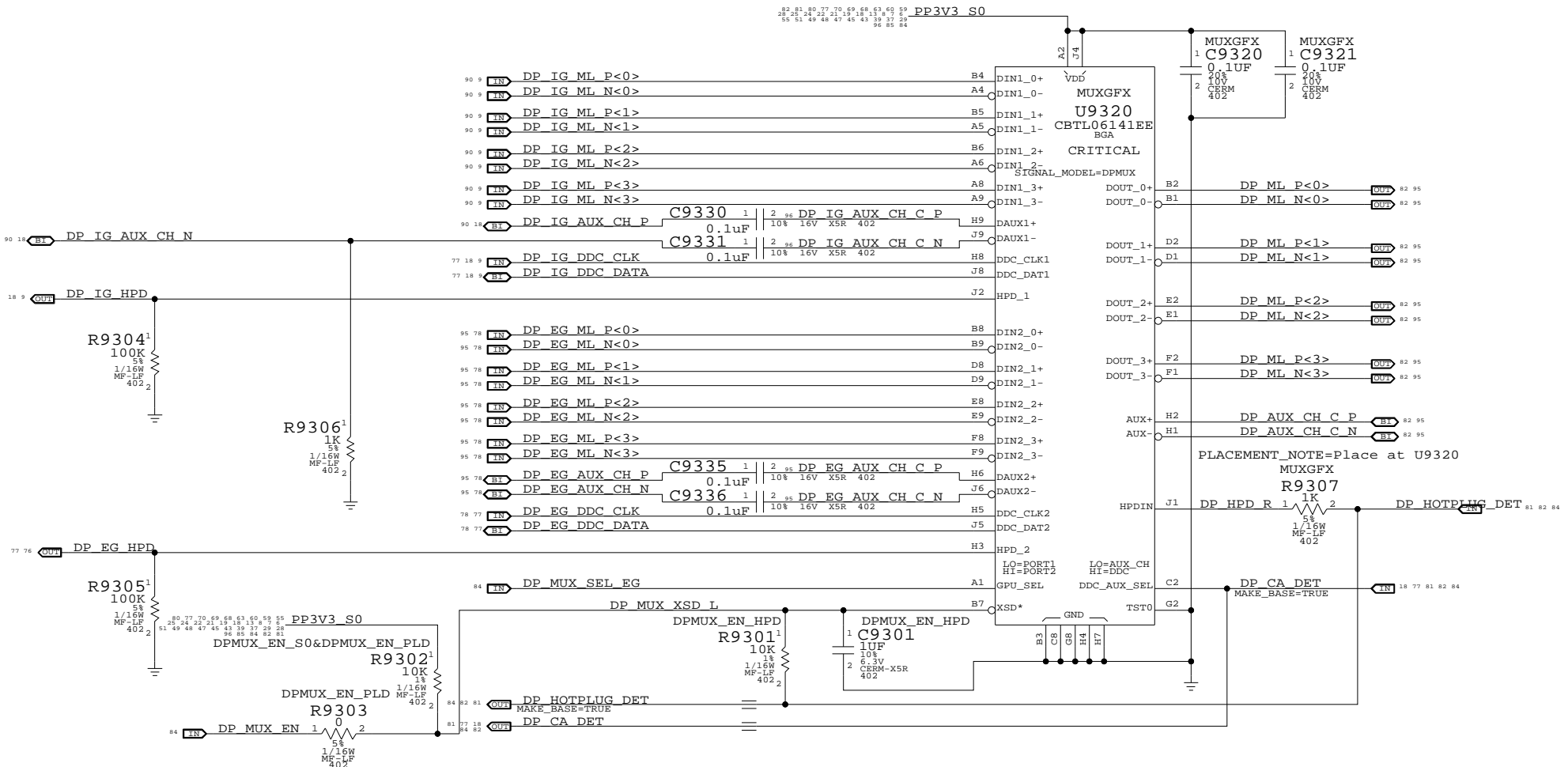
All emulated LVDS outputs require this termination

PLACEMENT NOTE=Place at U9600 (All 24 resistors)

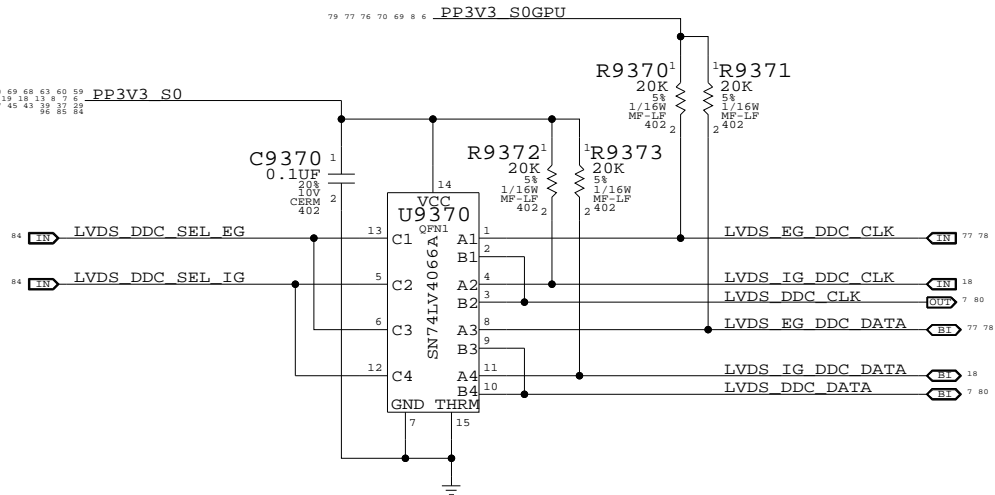


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0517	16	RES,MTL FILM,270 OHM,1%,1/16W,0402,SMD,L	R9320,R9321,R9322,R9325,R9326,R9327,R9330,R9331,R9332,R9335,R9336,R9337,R9340,R9341,R9342,R9345,R9346,R9347,R9350,R9351,R9352,R9355,R9356,R9357		GMUX_2V5
114S0174	16	RES,MTL FILM,1/16W,357 OHM,1%,0402,SMD,L	R9323,R9324,R9328,R9329,R9333,R9334,R9338,R9339,R9343,R9344,R9348,R9349,R9353,R9354,R9358,R9359		GMUX_1V8

DisplayPort Mux



LVDS DDC MUX

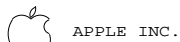


Muxed Graphics Support

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=12/05/2008

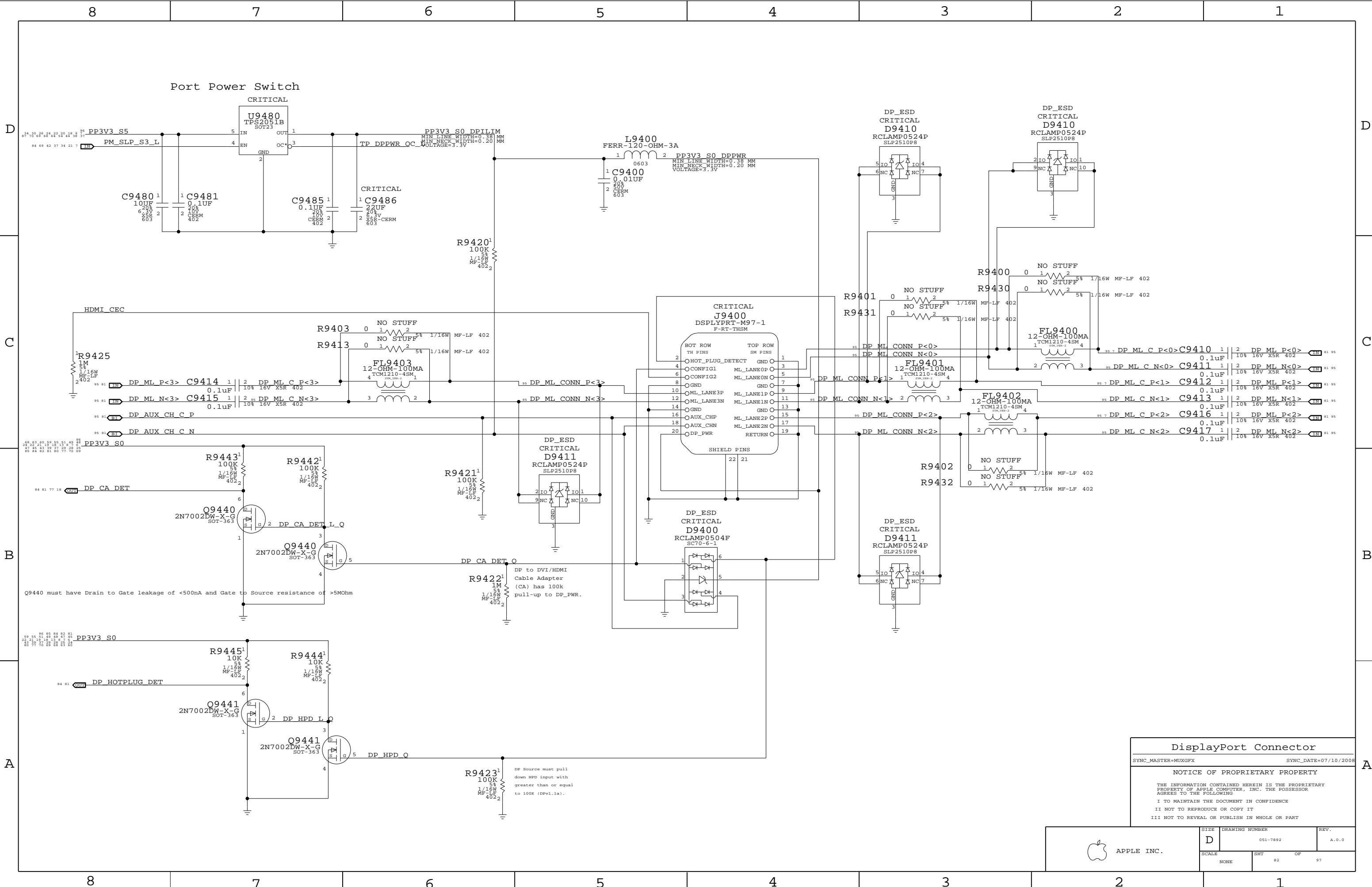
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NONE	81	97



DisplayPort Connector

SYNC_MASTER=MUXGFX

SYNC_DATE=07/10/2008

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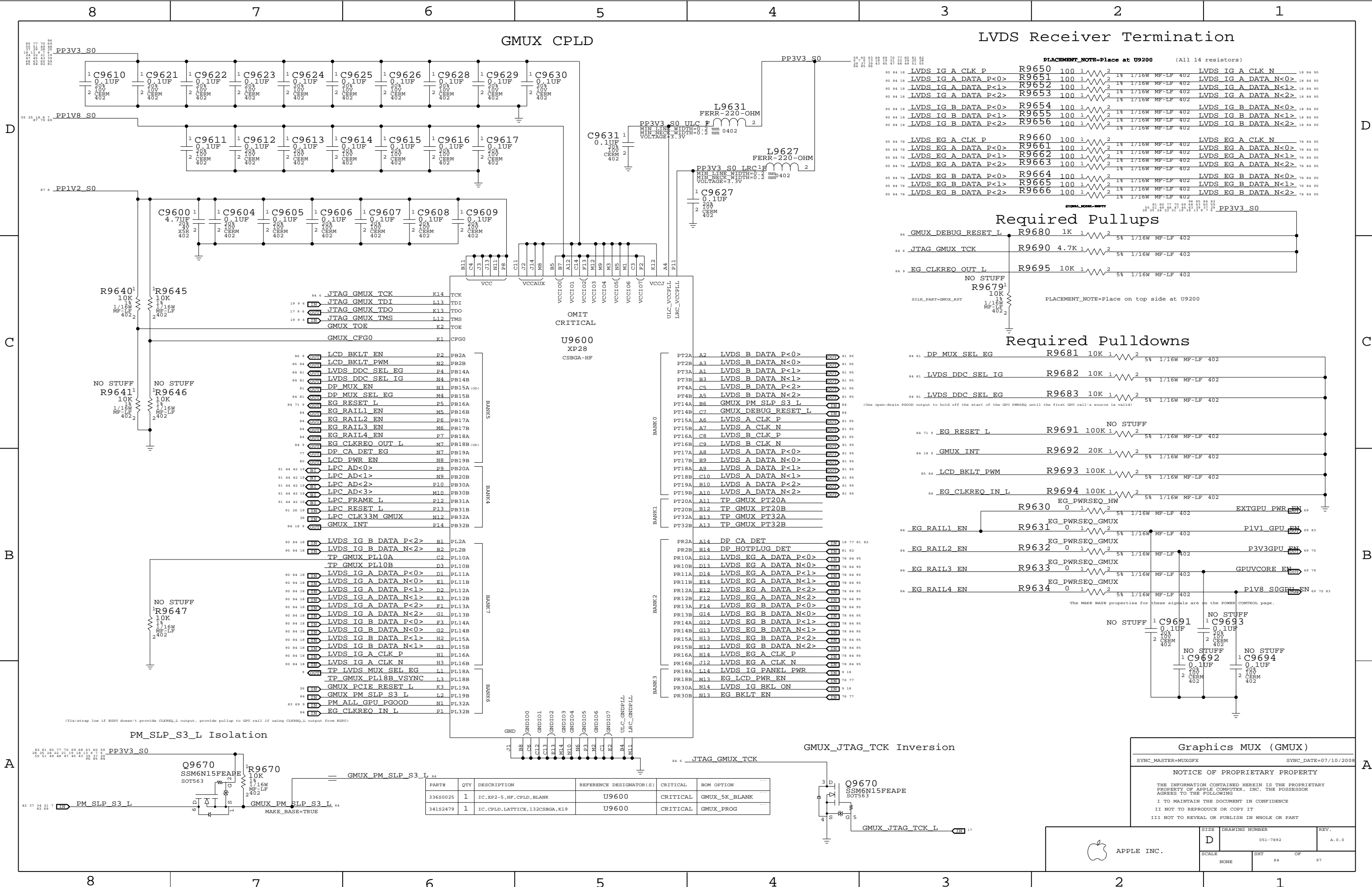
SHT

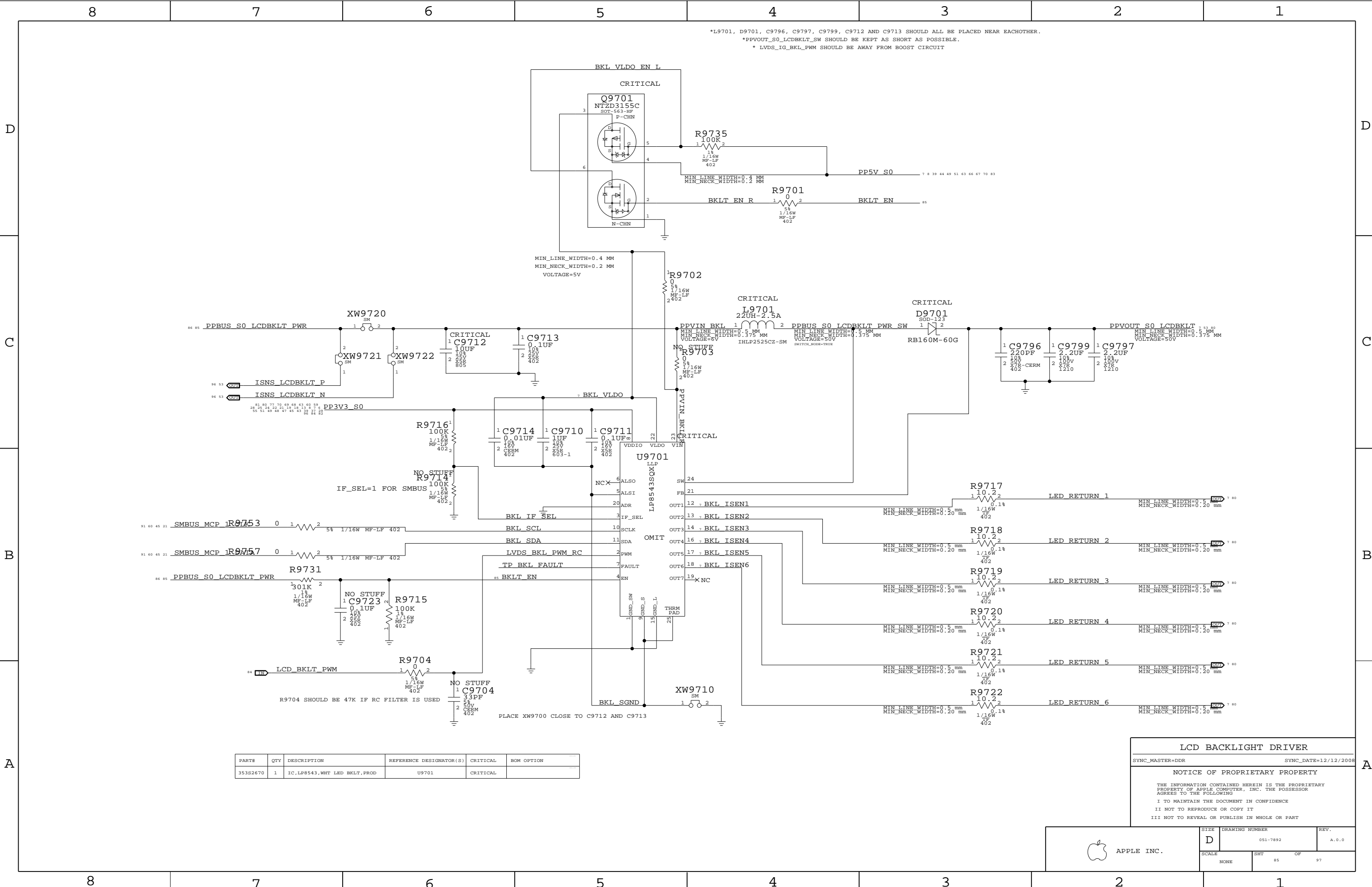
82

OF

97







PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2670	1	IC,LP8543,WHT LED BKL7,PROD	U9701	CRITICAL	

LCD BACKLIGHT DRIVER

SYNC_MASTER=DDR

SYNC_DATE=12/12/2008

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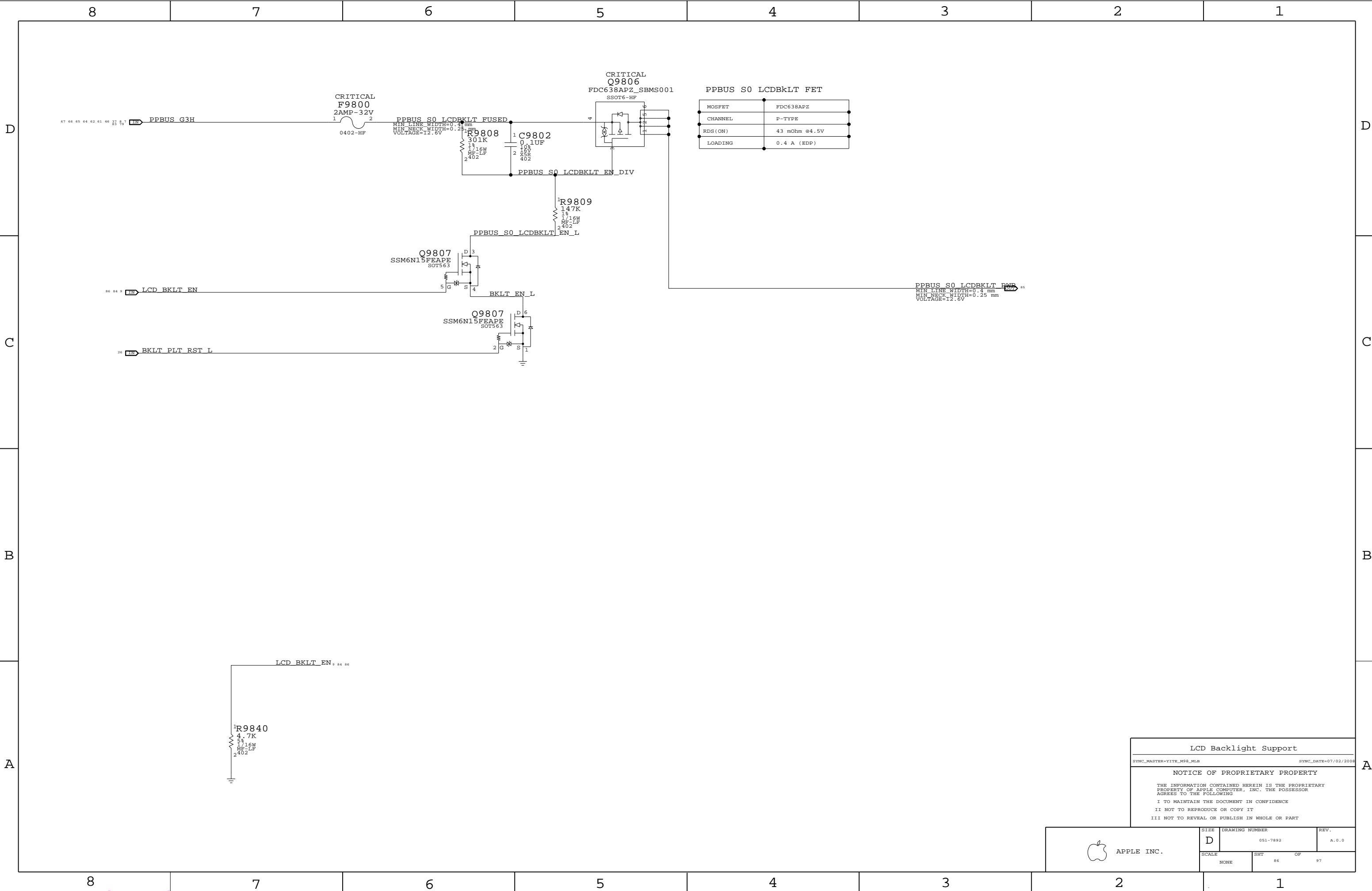
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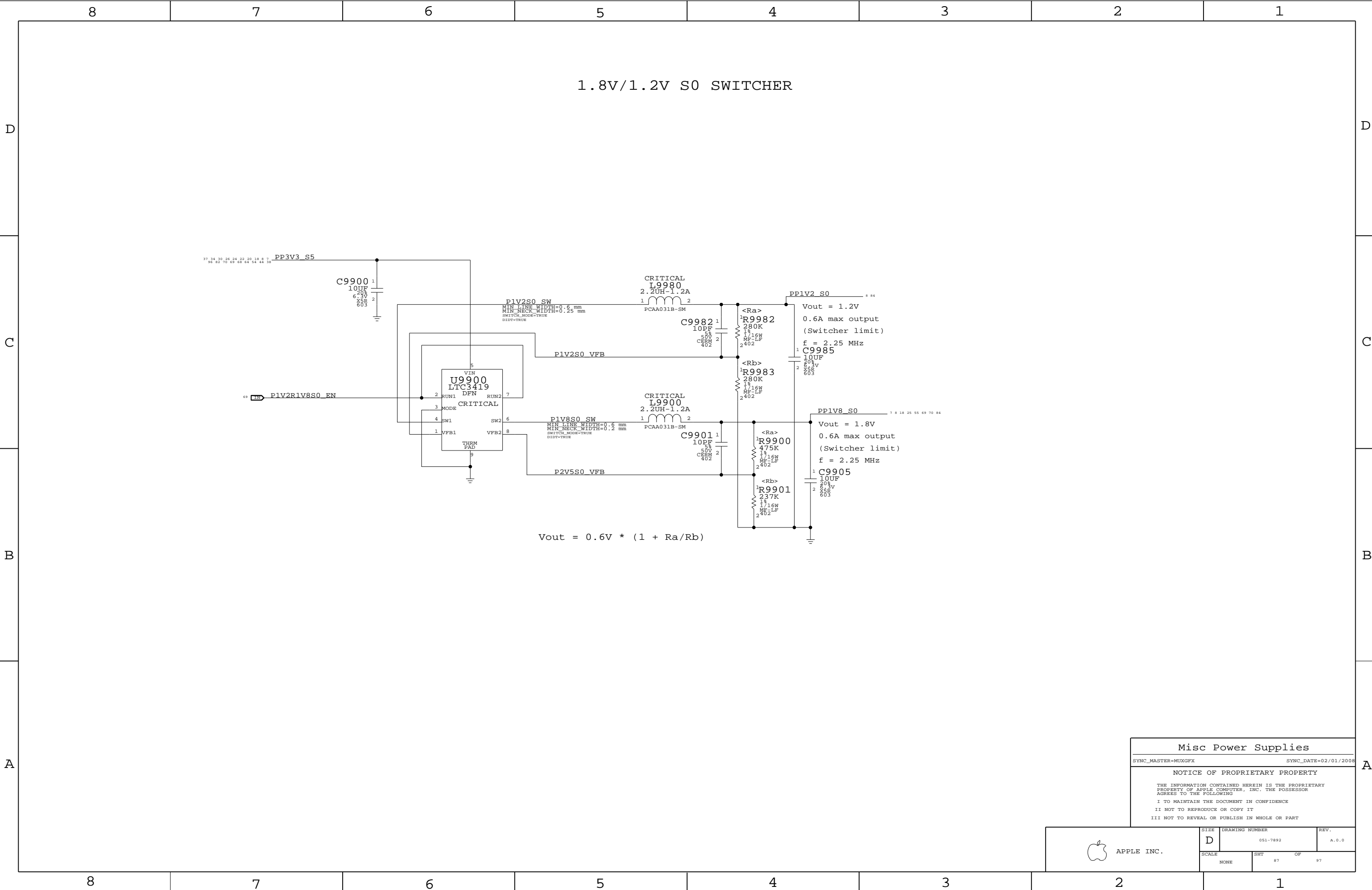
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NONE		85	97





Misc Power Supplies

SYNC_MASTER=MUXGFX SYNC_DATE=02/01/2008

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NONE		87	97

87654321

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.
Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

FSB 4X Signal Groups

FSB 2X Signals

FSB 1X Signals

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>	7 10 14
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>	7 10 14
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>	7 10 14
FSB_DSTR1	FSB_DSTR_50S	FSB_DSTR	FSB DSTB L P<1>	7 10 14
FSB_DSTR1	FSB_DSTR_50S	FSB_DSTR	FSB DSTB L N<1>	7 10 14
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>	7 10 14
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>	7 10 14
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>	7 10 14
FSB_DSTR3	FSB_DSTR_50S	FSB_DSTR	FSB DSTB L P<3>	7 10 14
FSB_DSTR3	FSB_DSTR_50S	FSB_DSTR	FSB DSTB L N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>	10 14
FSB_ADSTR0	FSB_50S	FSB_ADSTR	FSB ADSTB L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>	7 10 14
FSB_ADSTR1	FSB_50S	FSB_ADSTR	FSB ADSTB L<1>	7 10 14
FSB_1X	FSB_50S	FSB_1X	FSB ADS L	7 10 14
FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0 L	9 10 14
FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1 L	14
FSB_1X	FSB_50S	FSB_1X	FSB BNR L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB BPRI L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB DEFER L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB DRDY L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB HIT L	7 10 14
FSB_1X	FSB_50S	FSB_1X	FSB HITM L	7 10 14
FSB_1X	FSB_50S	FSB_1X	FSB LOCK L	7 10 14
FSB_CPURST_L	FSB_50S	FSB_1X	FSB CPURST L	9 10 13 14
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>	10 14
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L	10 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU A20M L	10 14
CPU_BSEL	CPU_50S	CPU_AGTL	CPU BSEL<2..0>	9 10
CPU_FERR_L	CPU_50S	CPU_8MIL	CPU FERR L	10 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU IGNNE L	10 14
CPU_INIT_L	CPU_50S	CPU_AGTL	CPU INIT L	10 14
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU INTR	9 10 14
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU NMI	9 10 14
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU PROCHOT L	10 14 43 63
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD	10 13 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU SMI L	10 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU STPCLK L	10 14
PM_THERMTRIP_L	CPU_50S	CPU_8MIL	PM THERMTRIP L	10 14 43
FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB CPUSLP L	10 14
CPU_FROM_SR	CPU_50S	CPU_AGTL	CPU DPSLP L	10 14
CPU_DPSTP_L	CPU_50S	CPU_AGTL	CPU DPRSTP L	9 10 14 63
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB DPWR L	10 14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	10 14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	10 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	13 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	13 14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	14
CPU_IERR_L	CPU_50S		CPU IERR L	10
PM_DPRSLEPVR	CPU_50S	CPU_AGTL	PM DPRSLEPVR	21 63
(See above)	CPU_50S	CPU_AGTL	IMVP DPRSLEPVR	63
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	10 27
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10
XDP_TDI	CPU_50S	CPU_ITP	XDP TDI	6 10 13
XDP_TDO	CPU_50S	CPU_ITP	XDP TDO	6 10
XDP_TMS	CPU_50S	CPU_ITP	XDP TMS	6 10 13
XDP_TCK	CPU_50S	CPU_ITP	XDP TCK	6 10 13
XDP_TRST_L	CPU_50S	CPU_ITP	XDP TRST L	6 10 13
XDP_BPM_L	CPU_50S	CPU_ITP	XDP BPM L<4..0>	10 13
XDP_BPM_L5	CPU_50S	CPU_ITP	XDP BPM L<5>	10 13
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP CPURST L	13
	CPU_50S	CPU_8MIL	CPU VID<6..0>	9 11
	CPU_50S	CPU_8MIL	IMVP6 VID<6..0>	9 63
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	11 63
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11 63
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P	63
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N	63

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CPU/FSB Constraints

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SYNC_DATE=02/18/2008

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	13.1 MM	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedance varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).
R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	?	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3X_DIELECTRIC	?
LVDS	*	=3X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4X_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4X_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4X_DIELECTRIC	?
SATA_TERM	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET

	NET_TYPE		
	PHYSICAL	SPACING	
	PCIE_90D	PCIE	PEG R2D P<15..0>
	PCIE_90D	PCIE	PEG R2D N<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C P<15..0>
	PCIE_90D	PCIE	PEG R2D C N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R P<15..0>
	PCIE_90D	PCIE	PEG D2R N<15..0>
	PCIE_90D	PCIE	PEG D2R C P<15..0>
	PCIE_90D	PCIE	PEG D2R C N<15..0>
	PCIE_90D	PCIE	PCIE MINI R2D P
	PCIE_90D	PCIE	PCIE MINI R2D N
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE MINI R2D C P
	PCIE_90D	PCIE	PCIE MINI R2D C N
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE MINI D2R P
	PCIE_90D	PCIE	PCIE MINI D2R N
	PCIE_90D	PCIE	PCIE FW R2D P
	PCIE_90D	PCIE	PCIE FW R2D N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D C P
	PCIE_90D	PCIE	PCIE FW R2D C N
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R P
	PCIE_90D	PCIE	PCIE FW D2R N
	PCIE_90D	PCIE	PCIE FW D2R C P
	PCIE_90D	PCIE	PCIE FW D2R C N
	PCIE_90D	PCIE	PCIE EXCARD R2D P
	PCIE_90D	PCIE	PCIE EXCARD R2D N
PCIE_EXCARD_R2D	PCIE_90D	PCIE	TP PCIE EXCARD R2D C P
	PCIE_90D	PCIE	TP PCIE EXCARD R2D C N
PCIE_EXCARD_D2R	PCIE_90D	PCIE	TP PCIE EXCARD D2R P
	PCIE_90D	PCIE	TP PCIE EXCARD D2R N
MCP_PE0_REECLK	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M P
	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M N
MCP_PE1_REECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI N
MCP_PE2_REECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW N
MCP_PE3_REECLK	CLK_PCIE_100D	CLK_PCIE	TP PCIE CLK100M EXCARD P
	CLK_PCIE_100D	CLK_PCIE	TP PCIE CLK100M EXCARD N
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP PEX CLK COMP
CRT_RED	CRT_50S	CRT	NC CRT IG R C PR
CRT_GREEN	CRT_50S	CRT	NC CRT IG G Y Y
CRT_BLUE	CRT_50S	CRT	NC CRT IG B COMP PB
CRT_SYNC	CRT_50S	CRT_SYNC	NC CRT IG HSYNC
CRT_SYNC	CRT_50S	CRT_SYNC	NC CRT IG VSYNC
MCP_DAC_RSET		MCP_DAC_COMP	NC MCP TV DAC RSET
MCP_DAC_VREF		MCP_DAC_COMP	NC MCP TV DAC VREF
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS IG TXC P
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS IG TXC N
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS IG TXD P<2..0>
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS IG TXD N<2..0>
DP_ML	DP_100D	DISPLAYPORT	DP IG ML P<3..0>
DP_ML	DP_100D	DISPLAYPORT	DP IG ML N<3..0>
DP_AUX_CH	DP_100D	DISPLAYPORT	DP IG AUX CH P
DP_AUX_CH	DP_100D	DISPLAYPORT	DP IG AUX CH N
MCP_HDMI_RSET	MCP_DV_COMP		MCP HDMI RSET
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP HDMI VPROBE
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK P
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK N
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA P<2..0>
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA N<2..0>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	NC LVDS IG A DATAP<3>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	NC LVDS IG A DATAN<3>
LVDS_IG_B_CLK	LVDS_100D	LVDS	NC LVDS IG B CLKP
LVDS_IG_B_CLK	LVDS_100D	LVDS	NC LVDS IG B CLKN
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA P<2..0>
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA N<2..0>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	NC LVDS IG B DATAP<3>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	NC LVDS IG B DATAN<3>
MCP_IFPAB_RSET	MCP_DV_COMP		MCP IFPAB RSET
MCP_IFPAB_VPROBE			MCP IFPAB VPROBE
SATA_HDD_R2D	SATA_100D	SATA	SATA HDD R2D C P
	SATA_100D	SATA	SATA HDD R2D C N
	SATA_100D	SATA	SATA HDD R2D P
	SATA_100D	SATA	SATA HDD R2D N
SATA_HDD_D2R	SATA_100D	SATA	SATA HDD D2R P
	SATA_100D	SATA	SATA HDD D2R N
	SATA_100D	SATA	SATA HDD D2R C P
	SATA_100D	SATA	SATA HDD D2R C N
SATA_ODD_R2D	SATA_100D	SATA	SATA ODD R2D C P
	SATA_100D	SATA	SATA ODD R2D C N
	SATA_100D	SATA	SATA ODD R2D P
	SATA_100D	SATA	SATA ODD R2D N
SATA_ODD_D2R	SATA_100D	SATA	SATA ODD D2R P
	SATA_100D	SATA	SATA ODD D2R N
	SATA_100D	SATA	SATA ODD D2R C P
	SATA_100D	SATA	SATA ODD D2R C N
MCP_SATA_TERM		SATA_TERM	MCP SATA_TERM

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MCP Constraints 1

SYNC_MASTER=MUXGFX

SYNC_DATE=02/18/2008

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4
88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL CONSTRAINT SETNET TYPEPHYSICALSPACINGMCP MII COMPVDD18MCP MII COMPGND18MCP CLK25M BUF0RTL8211 CLK25M CKXTAL118 34ENET_INTR_L18ENET_MDIO18ENET_MDC18ENET_PWRDN_L18ENET_CLK125M RXCLK_R33ENET_RXCLK33ENET_RXD<0>33ENET_RXD_STRAP18ENET_RX_CTRL18ENET_TXCLK18ENET_TXD<0>18ENET_TXD<3..1>18ENET_TX_CTRL18ENET_RESET_L18ENET_MDI_P<3..0>33ENET_MDI_N<3..0>33

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Ethernet Constraints

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?























SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

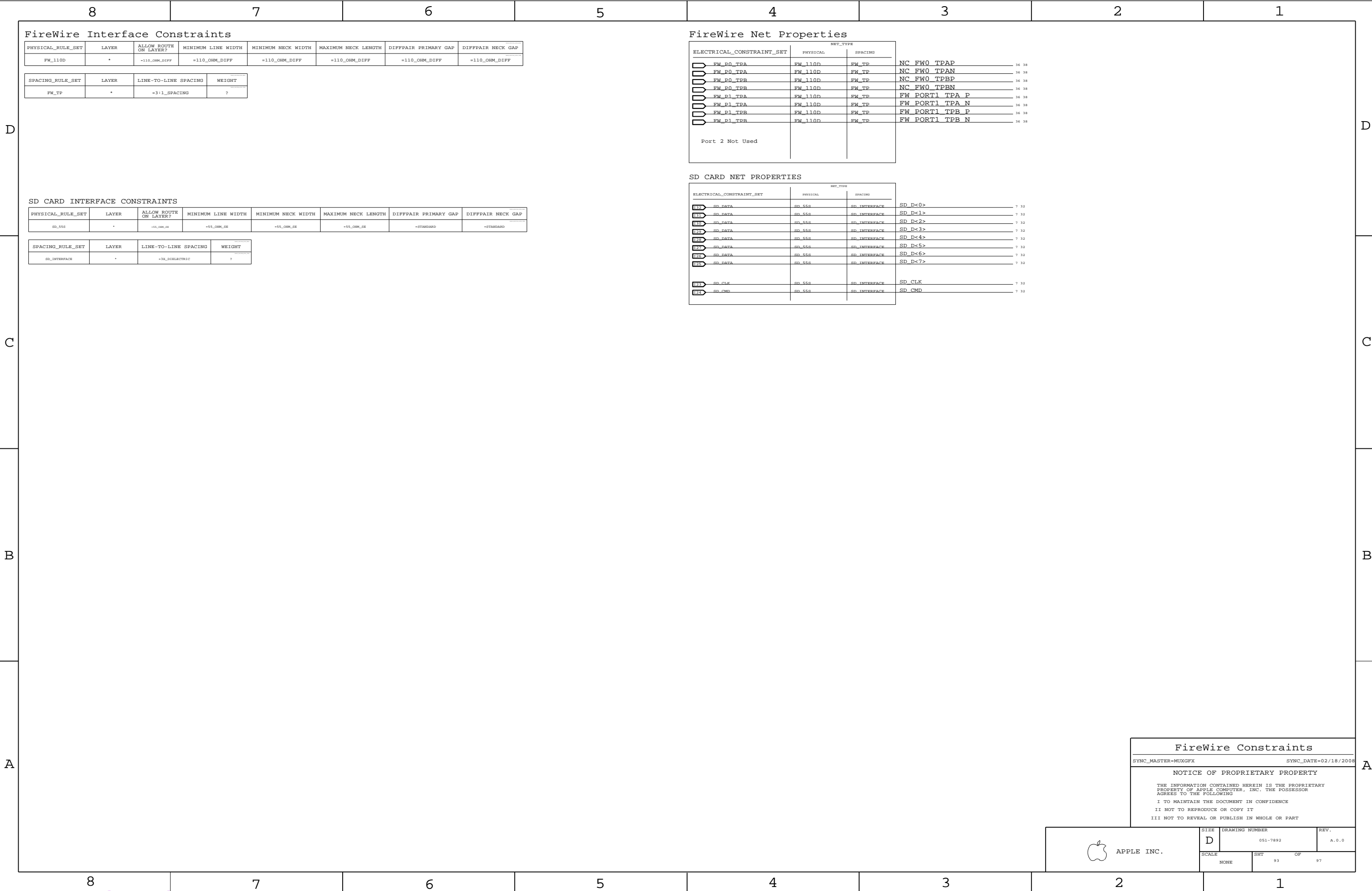
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		SPACING		
		PHYSICAL				
	MCP_MII_COMP	MCP_MII_COMP			MCP MII COMP VDD	18
	MCP_MII_COMP	MCP_MII_COMP			MCP MII COMP GND	18
	MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK		MCP CLK25M BUF0_R	18 34
		ENET_MII_55S	MCP_BUF0_CLK		RTL8211 CLK25M CKXTAL1	33 34
	ENET_INTR_L	ENET_MII_55S	ENET_MII		ENET INTR_L	
	ENET_MDIO	ENET_MII_55S	ENET_MII		ENET MDIO	18 33
	ENET_MDC	ENET_MII_55S	ENET_MII		ENET MDC	18 33
	ENET_PWDOWN_L	ENET_MII_55S	ENET_MII		ENET PWRDOWN_L	
		ENET_MII_55S	ENET_MII		ENET CLK125M RXCLK_R	33
	ENET_RXCLK	ENET_MII_55S	ENET_MII		ENET CLK125M RXCLK	18 33
		ENET_MII_55S	ENET_MII		ENET RXD R<3..0>	18 33
	ENET_RXD	ENET_MII_55S	ENET_MII		ENET RXD<0>	18 33
	ENET_RXD_STRAP	ENET_MII_55S	ENET_MII		ENET RXD<3..1>	18 33
	ENET_RXD	ENET_MII_55S	ENET_MII		ENET RX CTRL	18 33
		ENET_MII_55S	ENET_MII		ENET CLK125M TXCLK	18 33
	ENET_TXCLK	ENET_MII_55S	ENET_MII		ENET TXD<0>	18 33
	ENET_TXD0	ENET_MII_55S	ENET_MII		ENET TXD<3..1>	18 33
	ENET_TXD	ENET_MII_55S	ENET_MII		ENET TX CTRL	18 33
	ENET_TXD	ENET_MII_55S	ENET_MII		ENET RESET_L	18 33
		ENET_MII_55S	ENET_MII		ENET MDI P<3..0>	33 36
	ENET_MDI	ENET_MDI_100H	ENET_MDI		ENET MDI N<3..0>	33 36
		ENET_MDI_100H	ENET_MDI			

Ethernet Constraints			
SYNC_MASTER=MUXGFX		SYNC_DATE=02/18/2008	
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NONE		92	97





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GDDR3 Frame Buffer Signal Constraints															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
GDDR3_40R55SE		*	+45_OHM_SE	+40_OHM_SE	0.095 MM	12.7 MM	-STANDARD	-STANDARD							
GDDR3_40SE		*	+40_OHM_SE	+40_OHM_SE	0.095 MM	+40_OHM_SE	-STANDARD	-STANDARD							
GDDR3_80D		*	+40_OHM_DIFF	+40_OHM_DIFF	0.095 MM	+40_OHM_DIFF	+40_OHM_DIFF	+40_OHM_DIFF							
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT											
GDDR3_CLK		*	+2.5:1_SPACING	?											
GDDR3_CMD		*	+2.5:1_SPACING	?											
GDDR3_DATA		*	+2.5:1_SPACING	?											
GDDR3_DQS		*	+2.5:1_SPACING	?											
From T18 MXM:															
Digital Video Signal Constraints															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
DP_100D		*	+100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF							
LVDS_100D		*	+100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF							
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT											
DISPLAYPORT		*	=3x_DIELECTRIC	?											
LVDS		*	=3x_DIELECTRIC	?											
LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length. DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps. DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals. Max length of LVDS/DisplayPort/TMDS traces: 12 inches. SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.															
MUXGFX Net Properties															
ELECTRICAL_CONSTRAINT_SET		NET_TYPE		SPACING											
LVDS_A_CLK		LVDS_100D	LVDS	LVDS A CLK P											
LVDS_A_CLK		LVDS_100D	LVDS	LVDS A CLK N											
LVDS_A_DATA		LVDS_100D	LVDS	LVDS A DATA P<2..0>											
LVDS_A_DATA		LVDS_100D	LVDS	LVDS A DATA N<2..0>											
LVDS_B_CLK		LVDS_100D	LVDS	LVDS B CLK P											
LVDS_B_CLK		LVDS_100D	LVDS	LVDS B CLK N											
LVDS_B_DATA		LVDS_100D	LVDS	LVDS B DATA P<2..0>											
LVDS_B_DATA		LVDS_100D	LVDS	LVDS B DATA N<2..0>											
LVDS_CONN_A_CLK_F_P		LVDS_100D	LVDS	LVDS CONN A CLK F P											
LVDS_CONN_A_CLK_F_N		LVDS_100D	LVDS	LVDS CONN A CLK F N											
LVDS_CONN_B_CLK_F_P		LVDS_100D	LVDS	LVDS CONN B CLK F P											
LVDS_CONN_B_CLK_F_N		LVDS_100D	LVDS	LVDS CONN B CLK F N											
LVDS_CONN_A_CLK_P		LVDS_100D	LVDS	LVDS CONN A CLK P											
LVDS_CONN_A_CLK_N		LVDS_100D	LVDS	LVDS CONN A CLK N											
LVDS_CONN_A_DATA_P<2..0>		LVDS_100D	LVDS	LVDS CONN A DATA P<2..0>											
LVDS_CONN_A_DATA_N<2..0>		LVDS_100D	LVDS	LVDS CONN A DATA N<2..0>											
LVDS_CONN_B_CLK_P		LVDS_100D	LVDS	LVDS CONN B CLK P											
LVDS_CONN_B_CLK_N		LVDS_100D	LVDS	LVDS CONN B CLK N											
LVDS_CONN_B_DATA_P<2..0>		LVDS_100D	LVDS	LVDS CONN B DATA P<2..0>											
LVDS_CONN_B_DATA_N<2..0>		LVDS_100D	LVDS	LVDS CONN B DATA N<2..0>											
DP_ML		DP_100D	DISPLAYPORT	DP ML C P<3..0>											
DP_ML		DP_100D	DISPLAYPORT	DP ML C N<3..0>											
DP_ML		DP_100D	DISPLAYPORT	DP ML C P<3>.0>											
DP_ML		DP_100D	DISPLAYPORT	DP ML C N<3>.0>											
DP_ML		DP_100D	DISPLAYPORT	DP ML CONN P<3..0>											
DP_ML		DP_100D	DISPLAYPORT	DP ML CONN N<3..0>											
DP_AUX_CH		DP_100D	DISPLAYPORT	DP AUX CH C P											
DP_AUX_CH		DP_100D	DISPLAYPORT	DP AUX CH C N											
GPU (G96) CONSTRAINTS															
SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008															
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	+1:1_DIFFPAIR	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR
THERM_1T01_55S	*	+1:1_DIFFPAIR	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR
DIFFPAIR	*	+1:1_DIFFPAIR			+1:1_DIFFPAIR	+1:1_DIFFPAIR	+1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	+2:1_SPACING	?
THERM	*	+2:1_SPACING	?
AUDIO	*	+2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	+STANDARD	?
PP1V8_MEM	*	+STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P20M	*	0.20 MM	1000
PWR_P20M	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P20M
MEM_CMD	GND	*	GND_P20M
MEM_CTRL	GND	*	GND_P20M
MEM_DATA	GND	*	GND_P20M
MEM_DQS	GND	*	GND_P20M

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P20M
PCIE	GND	*	GND_P20M
SATA	GND	*	GND_P20M
USB	GND	*	GND_P20M
CLK_PCIE	SB_POWER	*	PWR_P20M
SATA	SB_POWER	*	PWR_P20M
USB	SB_POWER	*	PWR_P20M

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P20M

NET_SPACING_TYPE1NET_SPACING_TYPE2AREA_TYPESPACING_RULE_SET

CLK_PSBGND*GND_P20M

CPU_COMPGND*GND_P20M

CPU_GTLREFGND*GND_P20M

CPU_VCCSENSEGND*GND_P20M

PSB_D0TBPSB_D0TB*GND_P20M

NET_SPACING_TYPE1NET_SPACING_TYPE2AREA_TYPESPACING_RULE_SET

ENET_MDIGND*GND_P20M

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
DP_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

PGA CONSTRAINT RELAXATIONS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PGA_50SE	*	Y	+50_OHM_SE	0.073 MM	+50_OHM_SE	+1:1_DIFFPAIR	0.073 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PSB_50S	PGA	PGA_50SE
PSB_D0TB_50S	PGA	PGA_50SE
CPU_50S	PGA	PGA_50SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PSB_DATA	*	PGA	PGA_CPU
PSB_D0TB	*	PGA	PGA_CPU
PSB_ADDR	*	PGA	PGA_CPU
PSB_AD0TB	*	PGA	PGA_CPU
PSB_LX	*	PGA	PGA_CPU
CPU_A0TL	*	PGA	PGA_CPU
CPU_B0TL	*	PGA	PGA_CPU

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S_OVERRIDE	*	VERRIDE	VERRIDE	0.09 MM_OVERRIDE	5.8 MM_OVERRIDE	VERRIDE	VERRIDE
MEM_40S_VDD_OVERRIDE	*	VERRIDE	VERRIDE	0.09 MM_OVERRIDE	5.8 MM_OVERRIDE	VERRIDE	VERRIDE
MEM_70D_OVERRIDE	*	VERRIDE	VERRIDE	0.09 MM_OVERRIDE	5.8 MM_OVERRIDE	VERRIDE	VERRIDE
MEM_70D_VDD_OVERRIDE	*	VERRIDE	VERRIDE	0.09 MM_OVERRIDE	100 MIL_OVERRIDE	VERRIDE	VERRIDE
PCIE_90D_OVERRIDE	*	VERRIDE	VERRIDE	0.09 MM_OVERRIDE	100 MIL_OVERRIDE	VERRIDE	VERRIDE
USB_90D_OVERRIDE	*	VERRIDE	VERRIDE	0.09 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_DV_COMP_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_MEM_COMP_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_MIL_COMP_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_USB_RBIAS_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_DV_COMP_OVERRIDE	*_OVERRIDE	VERRIDE	VERRIDE	0.25 MM_OVERRIDE	250 MIL_OVERRIDE	VERRIDE	VERRIDE
CPU_27P4S_OVERRIDE	BOTTOM_OVERRIDE	VERRIDE	VERRIDE	0.23 MM_OVERRIDE	100 MIL_OVERRIDE	VERRIDE	VERRIDE

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S_OVERRIDE	ISL4, ISL9_OVERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE
MEM_40S_VDD_OVERRIDE	ISL3, ISL10_OVERRIDE	N_OVERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE
MEM_70D_OVERRIDE	ISL4, ISL9_OVERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE
MEM_70D_VDD_OVERRIDE	ISL3, ISL10_OVERRIDE	N_OVERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE

Ground-referenced memory signals (DQ,DQM,DQS) MAY route on ISL9 (VDD-referenced plane)but not next to VDD island.
Forces power-referenced memory signals (CLK,ADDR,CTRL) to not route on ISL3, ISL4 & ISL10(GND-referenced planes).

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S_OVERRIDE	ISL4, ISL9_OVERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE
MEM_40S_VDD_OVERRIDE	ISL3, ISL10_OVERRIDE	N_OVERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE
MEM_70D_OVERRIDE	ISL4, ISL9_OVERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE
MEM_70D_VDD_OVERRIDE	ISL3, ISL10_OVERRIDE	N_OVERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE

Project Specific Constraints

SYNC_MASTER=MUXGFXSYNC_DATE=02/21/2008

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SCALE: NONE

DRAWING NUMBER: 051-7892

SHT: 96

OF: 97

REV: A.0.0

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S_OVERRIDE	*	VERRIDE	VERRIDE	0.09 MM_OVERRIDE	5.8 MM_OVERRIDE	VERRIDE	VERRIDE
MEM_40S_VDD_OVERRIDE	*	VERRIDE	VERRIDE	0.09 MM_OVERRIDE	5.8 MM_OVERRIDE	VERRIDE	VERRIDE
MEM_70D_OVERRIDE	*	VERRIDE	VERRIDE	0.09 MM_OVERRIDE	5.8 MM_OVERRIDE	VERRIDE	VERRIDE
MEM_70D_VDD_OVERRIDE	*	VERRIDE	VERRIDE	0.09 MM_OVERRIDE	100 MIL_OVERRIDE	VERRIDE	VERRIDE
PCIE_90D_OVERRIDE	*	VERRIDE	VERRIDE	0.09 MM_OVERRIDE	100 MIL_OVERRIDE	VERRIDE	VERRIDE
USB_90D_OVERRIDE	*	VERRIDE	VERRIDE	0.09 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_DV_COMP_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_MEM_COMP_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_MIL_COMP_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_USB_RBIAS_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_DV_COMP_OVERRIDE	*_OVERRIDE	VERRIDE	VERRIDE	0.25 MM_OVERRIDE	250 MIL_OVERRIDE	VERRIDE	VERRIDE
CPU_27P4S_OVERRIDE	BOTTOM_OVERRIDE	VERRIDE	VERRIDE	0.23 MM_OVERRIDE	100 MIL_OVERRIDE	VERRIDE	VERRIDE

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S_OVERRIDE	ISL4, ISL9_OVERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE
MEM_40S_VDD_OVERRIDE	ISL3, ISL10_OVERRIDE	N_OVERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE
MEM_70D_OVERRIDE	ISL4, ISL9_OVERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE
MEM_70D_VDD_OVERRIDE	ISL3, ISL10_OVERRIDE	N_OVERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE	VERRIDE

Project Specific Constraints

SYNC_MASTER=MUXGFXSYNC_DATE=02/21/2008

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SCALE: NONE

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	8	7	6	5	4	3	2	1
D	K19 Board-Specific Spacing & Physical Constraints							
	BOARD LAYERS			BOARD AREAS		BOARD UNITS (MIL or MM)	ALLEGRO VERSION	
	TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NOLTYPE, BGA, PGA		MM	15.5.1	
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
C	DEFAULT	*	Y	>50_OHM_SE	>50_OHM_SE	33.6 MM	0 MM	0 MM
	STANDARD	*	Y	<DEFAULT	<DEFAULT	10 MM	<DEFAULT	<DEFAULT
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
B	55_OHM_SE	*	Y	0.076 MM	0.076 MM	<STANDARD	<STANDARD	<STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.095 MM			
	50_OHM_SE	*	Y	0.090 MM	0.090 MM	<STANDARD	<STANDARD	<STANDARD
A	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM			
	40_OHM_SE	*	Y	0.135 MM	0.135 MM	<STANDARD	<STANDARD	<STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.095 MM			
	27P4_OHM_SE	*	Y	0.250 MM	0.250 MM	<STANDARD	<STANDARD	<STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	70_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD
	70_OHM_DIFF	ISL3, ISL4	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
	70_OHM_DIFF	ISL9, ISL10	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
	70_OHM_DIFF	ISL2, ISL11	Y	0.170 MM	0.170 MM		0.150 MM	0.150 MM
	70_OHM_DIFF	TOP, BOTTOM	Y	0.170 MM	0.095 MM		0.150 MM	0.150 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	80_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD
	80_OHM_DIFF	ISL3, ISL4	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
	80_OHM_DIFF	ISL9, ISL10	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
	80_OHM_DIFF	ISL2, ISL11	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
	80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.095 MM		0.190 MM	0.190 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	90_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD
	90_OHM_DIFF	ISL3, ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
	90_OHM_DIFF	ISL9, ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
	90_OHM_DIFF	ISL2, ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM
	90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.095 MM		0.230 MM	0.230 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	100_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD
	100_OHM_DIFF	ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
	100_OHM_DIFF	ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
	100_OHM_DIFF	ISL2, ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
	100_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	110_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD
	110_OHM_DIFF	ISL3, ISL4	Y	0.077 MM	0.077 MM			